One of the most common pieces of equipment encountered in the semiconductor industry is the vacuum system. Such systems come in many varieties, and are designed to produce low pressures ranging from about $10^{-3}$ atmospheres to less than $10^{-12}$ atm. In our laboratory, we use a rotary vane mechanical pump to produce rough vacuums ($10^{-2} - 10^{-3}$ Torr, or 10 to 1 mTorr, where 1 atm = 760 Torr), and an oil diffusion pump to produce high vacuum ($10^{-6}$ Torr). These pumps work in conjunction to evacuate the bell jar which contains our metal evaporation source. Such low pressures are necessary to prevent the evaporating metal from oxidizing. It also allows the metal to go directly from source to chip without undergoing any collisions with residual gas molecules (the mean free path between collisions at $10^{-6}$ Torr is almost 50 meters, compared to 70 nanometers at 760 Torr). This helps to produce relatively pure, highly conducting metal layers.

The rough pump we use is shown in cross section in Figure 27. The pump consists of a spinning cylinder (the rotor) positioned off-center inside a larger cylinder (the stator). The rotor is precisely machined so it fits very closely against the stator at the top, while spring-loaded vanes make contact with the walls of the stator. When the rotor spins, gas is trapped in the cavity between the vanes, and is swept out the outlet valve. The outlet side of the pump is actually filled with oil so that all parts are covered with a thin layer of oil, which serves as both lubricant and gas seal.

![Rotating-vane two-stage rough pump](image)


To achieve lower pressures we use an oil diffusion pump, shown schematically in Figure 28. Here a very high purity, low boiling point oil is heated at the bottom of the pump. The hot vapors then rush up the chimney and are ejected downward from the jet assembly. Via collisions between the directed oil molecules and the residual gas
molecules, the gas is compressed and swept out the foreline, where it is pumped away by our rotary vane rough pump. The diffusion pump is water cooled to insure that any oil that strikes the pump walls will stick, rather than bouncing off and disturbing the gas flow. In addition, since it is inevitable that some oil will be deflected up towards the vacuum chamber, we interpose two baffles between the chamber and pump (see Figure 31). These baffles consist of cooled metal chevrons, which do not allow any line-of-sight paths to the chamber. Almost all oil molecules diffusing upward will collide and stick to one of these baffles. It is important to realize diffusion pumps work only at low pressures (below about 10 mTorr) where the mean free paths are fairly large. If the pump intake is exposed to high pressure (≥ 100 mTorr) for any length of time serious damage will result. At these pressures large amounts of oil will be carried into the process chamber, and the oil in the pump will begin to burn. Because of this the pressure in the foreline should never exceed about 500 mTorr (i.e., TC2 ≤ 500 mTorr in Fig. 3 at all times).

![Figure 28: Oil Diffusion Pump](image)

**Figure 28: Oil Diffusion Pump**

A cross sectional view of a metal-bodied diffusion pump and some of its innovations: (1) Cooled hood for prevention of vapor backstreaming; (2) heater for the nozzle’s cap to compensate for loss of heat; (3) streamlined surface to avoid turbulence; (4) multiple stages to obtain low pressures; (5) enlarged casing to give larger pumping aperture; (6) baffle to impede the access to the jet of liquid splashed up from the boiler; (7) heater for superheating the vapor; (8) lateral ejector stage; (9) conical body allowing operation against higher forepressures; (10) hot maintained diffuser for oil purification; (11) catchment and drain-off of highly volatile oil components; (12) baffle to reduce oil loss; (13) concentric chimneys that allow oil fractionation. Adapted from J. O’Hanlon, *A User's Guide to Vacuum Technology*. New York: John Wiley & Sons, 1980, p. 191.

We use two different types of gauges to measure the pressures in our vacuum system. The first is the thermocouple (TC) gauge (Figure 28), used to measure pressures greater than 1 mTorr. There are two TC gauges, one in the foreline (TC2 in Figure 31), and one on the bell jar (TC1 in Figure 31). The operating principle used by these gauges is the relation between gas pressure and gas thermal conductivity. They consist of a hot
filament surrounded by a cylinder. A thermocouple is used to measure the temperature of
the filament; as gas pressure increases, more heat is transferred from the filament to the
cylinder, and the thermocouple gauge output voltage registers the subsequent temperature
drop. Thermocouple gauges are quite rugged, and are widely used, although fairly
inaccurate.

Figure 28: Thermocouple gauge.

The second type of gauge used in our system is the ionization gauge (Figure 29). These
gauges are used to measure pressure from $10^{-10}$ Torr to 1 mTorr. They use high
voltage electron emission to measure pressure. The current which flows between the
gauge's anode and cathodes is related to the gas pressure, but not in a linear fashion.
These gauges are fairly accurate but are somewhat fragile. Due to the gauge location in
our system, the pressure registered is initially higher than that actually in the bell jar.

Figure 29: Bayard-Alpert ionization gauge. Adapted from J. O'Hanlon, A User's
Once a high vacuum has been established inside the bell jar, the actual metal deposition must still be done. Many different techniques are used in industry, but we use one of the oldest and simplest: resistive heating of the source material. The easiest way of doing this is to use a very high melting point material (such as tungsten) through which a large current is passed. This heater can be in many forms; three of the more common types are shown in Figure 31. The material to be evaporated (see Table 1 for examples) is simply placed in the heater. A variety of problems can be encountered with this technique. When evaporating aluminum, for example, it is found that molten Al is very reactive with the tungsten filament. For this reason we always use a minimum amount of Al, and try to evaporate all of the metal from the filament during each run. Table 1 summarizes many other metal/heater combinations that can be used for evaporations. Nomograph 1 and Table 2 allow the calculation of current necessary in a tungsten filament to achieve various evaporation rates. As a rule of thumb, a vapor pressure of about $10^{-2}$ Torr is necessary for a moderate evaporation rate of approximately 10 Å per second.

**Figure 30: Varian vacuum evaporation system used in our lab.**

**Figure 31: Resistance heated evaporation sources.**
Varian Vacuum System Operating Procedure (see Figure 31)

1. SIGN IN on log book. The vacuum sequence controller should be in the AUTO mode, with the STOP light lit.

2. Make sure the FORELINE valve is OPEN, ROUGHING valve CLOSED. Make sure the HIGH VAC valve is CLOSED. TC2 should read less than 10 mTorr.

3. The TA will open the BELL JAR VENT VALVE by depressing and holding in the STOP BUTTON on the front panel; continue to hold in the button until the bell jar is fully vented. TC2 should remain at less than 10 mTorr, and TC1 should rise very quickly to 1 atm.

   NOTE: If TC2 rises, IMMEDIATELY close the vent valve by releasing the STOP BUTTON and seek assistance.

4. After venting is complete check to make sure the bell jar is loose, and use the hoist to raise the jar. Remove the evaporation chimney CAREFULLY, and set it aside.

   NOTE: You MUST WEAR GLOVES when handling anything inside a vacuum system. Finger oil is one of the most offensive vacuum contaminates.

5. Load metal into filament: for aluminum, carefully wrap 3" to 4" of aluminum wire around the center of the filament; the wire must be wrapped only in about the central 1/8" of the filament. Check to make sure the filament has not broken: with the evaporation power supply variac set to zero, turn the supply on; then quickly turn up the variac, then turn it back off. The ammeter on the control panel should indicate current flow.

6. Mount chips on the sample holder and then replace chimney and sample holder. Be careful to not hit the Crystal Thickness Monitor, which is used to measure film thickness. Turn the Crystal Thickness Monitor ON, and zero it. Make sure the thickness monitor is working before you begin the pump-down cycle!

7. CAREFULLY lower the bell jar by reversing the hoist. If you hit the chimney while lowering the jar you may dislodge a sample, so be very careful.
8. After the jar is lowered and centered on the base plate make sure the bell jar VENT VALVE is closed.

9. Begin vacuum cycle by pressing the START button on the sequencer. The controller will now perform the following steps, while you monitor the items shown in bold-face print:

a) FORELINE valve CLOSED, pause, ROUGHING valve OPEN.

b) WATCH TC2 (foreline pressure) - it should remain stable, or rise ONLY VERY SLOWLY. TC2 MUST REMAIN ≤ 200 mTorr.

c) Watch TC1 (bell jar pressure); it should fall to ≤ 200 mTorr in about 2-3 minutes.

d) When TC1 reaches about 50 mTorr, the ROUGHING valve will CLOSE, and after a pause, the FORELINE valve will OPEN. TC1 (bell jar pressure) should remain constant or very slowly rise; TC2 (foreline pressure) should drop to less than 10 mTorr very quickly. After a brief pause, the HIGH VAC VALVE will now open.

e) Watch TC2: it should jump to about 100 mTorr, and then immediately begin to fall back towards 10 mTorr; TC1 should very quickly drop to zero.

f) Turn on ION GAUGE.

10. Wait 10-15 minutes. Check to see if LN$_2$ trap is cold (ask the TA). The ion gauge should read about 10$^{-6}$ Torr.

11. Evaporate metal:

a) Set current shunt to appropriate feedthroughs. Make sure Crystal Thickness Monitor is ON, and zeroed. Make sure shutter is CLOSED.

b) Make sure VARIAC is at ZERO, then turn on power supply. While watching through cracks above and below the chimney, turn VARIAC up until you see a glow.
c) Set CURRENT to evaporation level:
   Aluminum: about 50 Amps
   Gold: about 40 Amps
Wait about 10 seconds, then open shutter between the chips and the evaporation filament.

d) Watch the Thickness Monitor display; it should register the depositing metal, at a rate of around 10 Å/sec. After about 2 min. the rate should rapidly drop; you have now evaporated all the aluminum that was on the filament. NOTE THE THICKNESS DEPOSITED FOR LATER REFERENCE.

e) Close the shutter.

f) TURN VARIAC TO ZERO, power supply off.

12. Let samples cool under vacuum for 5 minutes. Turn ion gauge off.

13. Begin shut-down by pressing the STOP button:
   a) The HIGH VAC valve will close.

   b) While watching TC2, the TA will open the bell jar vent valve by pressing and holding the STOP button. TC2 SHOULD NOT CHANGE. If TC2 increases, immediately close the vent valve by releasing the STOP button; check to see if the HIGH VAC VALVE IS CLOSED.

   c) Continue venting by holding in the STOP button until jar is at atmosphere.

   d) Remove samples.

14. Vacuum System standby:

   Repeat steps 7, 8 and 9, but IMMEDIATELY AFTER THE HIGH VAC VALVE OPENS, PRESS STOP. DO NOT VENT THE BELL JAR.
When you leave the system the valves should be set as follows:

HIGH VAC VALVE CLOSED.
FORELINE VALVE OPEN.
BELL JAR VENT VALVE CLOSED.

The gauges should read as follows:

TC2 (foreline pressure) ≤ 10 mTorr
TC1 (bell jar pressure) ≤ 100 mTorr
ION GAUGE OFF.
The resistivity, $\rho$, of a sample is an important parameter, since it can be related to impurity concentration (to characterize a doping process, for example), as well as having direct effects on device performance. A simple, nondestructive way of determining $\rho$ utilizes the four point probe, shown schematically in Figure 32. Here four sharply tipped tungsten wires (tungsten is chosen for its hardness) are brought into contact with the semiconductor surface. One immediate problem arises from the contact between the metal and the silicon. At the very least, the Schottky diodes formed there make it impossible to measure resistance using a simple ohm meter and only two connections.

**Figure 32:** Four point probe; sample dimensions and orientation of probe refer to Table 13.

The four point probe avoids this problem by using a row of four equally spaced needles. A known current is passed between the outer needles, while an open-circuit voltage reading is made between the inner needles. Because no (or very little) current flows through the voltage sensing needles, there are no errors introduced due to the contacts. Of course, there are large voltage drops across the outside needle contacts, but we measure only current in this part of the circuit.
We are faced with another difficulty, however, in extracting the resistivity from the measured $I$ and $V$. Here the current-carrying probes (outer probes) represent a dipole source, which establishes a field distribution inside the specimen under test. We must solve for the potential difference between the two inner probes under various boundary conditions, set by the sample size and thickness, to derive expressions relating the supplied current, the measured potential difference, and the resistivity of the specimen.

In two limiting cases it is relatively straightforward to find these expressions. For a semi-infinite sample the resistivity is given by

$$\rho = \frac{(2\pi s)V}{I}$$

(1)

where the probes are assumed to be equally spaced by $s$ (ref.1).

The second case is somewhat more useful, the "thin" two-dimensional conducting sheet. Here the current is assumed to be completely confined to a layer $t$ thick, where $t$ is thin, i.e., $t \ll s$. For such sheets it is convenient to define the "Sheet Resistance", $R_S$, in ohms/square, or $\Omega/\square$. This is simply the resistance of a bar of material of unit length and width, with thickness $t$. Clearly if $t$ is known, then

$$\rho = R_S t \ (\Omega-cm)$$

(2)

and for the two-dimensional sheet (ref. 2),

$$R_S = \frac{\pi}{ln2} \frac{V}{I} = 4.53 \frac{V}{I} \ (\Omega/\square)$$

(3)

In the case of a sample which has been doped by a diffusion process, the resistivity of the diffused layer is much lower than the substrate, which confines almost all the current to this layer (or if the diffusion is of opposite type to the substrate the resulting p-n junction serves to block current from flowing into the substrate), and the requirement $t \ll s$ is easily satisfied. Also note that since the depth of the diffusion, $t$, must be determined in some other manner, it is common to give only the sheet resistance, $R_S$. When $t$ is known eqs 2 and 3 give

$$\rho = 4.53 t \ \frac{V}{I} \ (\Omega-cm)$$

(4)

In the above cases, no edge effects have been considered, and the calculated potential distributions are due to a single dipole source only. For a real sample of finite size, however, the edge effects cannot be ignored. The so-called "diameter" correction factor, $CF_d$, and "thickness" correction factor, $CF_t$, have to be considered separately to account for finite sample size. The method of images can be used here to solve for the potential in the presence of finite boundaries. The basic principle is to remove the edges by mirror-imaging the dipole source through the imaginary edge plane, and treat the whole problem in a single medium. As a result, a single dipole source is now replaced by an infinite arrangement of dipoles. Once again, the potential difference between the inner
probes due to these infinite dipoles can be solved numerically. The resulting diameter and thickness correction factors are given in tables 1 and 2. The bulk resistivity and sheet resistance for a real sample can thus be expressed in final form as

\[ \rho = \frac{V}{I} t CF_d CF_t \]

and

\[ R_s = \frac{V}{I} CF_d CF_t \]

For any epitaxial or diffusion layer in our lab, \( t/s < 0.5 \), and \( CF_t = 1 \). In fact, the thickest conductive layer we encounter is our wafer substrate, \( t \leq 0.025" \). Our probe spacing \( s = 0.040" \), so even for a bare wafer, \( t/s \leq 0.625 \), and \( CF_t \geq 0.9898 \). Note, however, that for many of our samples the diameter correction factor, \( CF_d \), cannot be set to its limiting value of 4.53.

MEASURING PROCEDURES

1. Measure dimensions of the specimen. The probe head tip spacing \( s \) is 0.040". Estimate correction factors \( CF_d \) and \( CF_t \).

2. Turn the HP current source on by setting the Function Selector switch to DC. Make sure the Output Switch is set to the OFF position (this is a center off switch). The initial Range setting should be 0.1mA, and the Current Multiplier Dial should be set at 0.500.

3. Place specimen on insulated vacuum chuck, turn on vacuum, and locate sample under probe head. Lower probe head by pressing front lever down until it stops. Make sure the current source Output Switch is OFF before lowering the probe head onto the wafer. The probe tips should retract at least 0.040" into the head after contact is made. Lock head down with the locking screw on the left side of the prober.

NOTE: The probe head is a precision made instrument! Care must be exercised--no excessive force should be exerted. Actual contact is maintained via springs internal to the probe head to insure repeatable contact pressures.

NOTE: THE MEASUREMENTS MADE BELOW MAY EXHIBIT SIGNIFICANT DEPENDENCE ON ILLUMINATION. YOU SHOULD TRY TURNING OFF THE ROOM LIGHTS TO DETERMINE IF YOUR SAMPLES ARE SENSITIVE; IF SO, MAKE MEASUREMENTS IN THE DARK.
4. Set current range to obtain a voltage reading of between 15 and 20 mV:

   i) To apply a current to the sample depress and continue to hold down the Output Selector switch to the ON TEST position (this is a momentary contact switch; when you release it the Output Selector switch returns to the OFF position).

   ii) Read volt meter; if

       a) \( V \leq 2\text{mV} \), release Output Selector switch, change the Range selector to the next higher decade, and read volt meter again

       b) \( V \leq 2\text{mV} \), repeat step (i) and (iia) above until

       c) \( 2\text{mV} \leq V \leq 15\text{mV} \), adjust the Multiplier Dial until

       d) \( 15\text{mV} \leq V \leq 20\text{mV} \), record \( V \) and I.

5. Reverse the polarity of the current by reversing the banana plug connections to the current supply, and repeat step 4. Make sure the Output Selector is OFF before reversing the polarity.

6. If the "positive" and "negative" measurements above are within approximately 4% of each other, you can assume confidence in the readings. If not, see your TA.

7. Average readings from 4 and 5, and using correction factors calculate \( R_s \) and \( \rho \) (if \( t \) is known).

8. Make sure the Output Selector is OFF before raising the probe head from the sample. Serious damage to the probe head may result if the current source is still applied to the sample when the head is raised!
### Table 13: Diameter Correction Factor $C_{F_d}$ (after ref. 2)

<table>
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<tr>
<th>$d/s$</th>
<th>CIRCLE 1</th>
<th>2</th>
<th>3</th>
<th>$\geq 4$</th>
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<td>1.0</td>
<td>0.998</td>
<td>0.999</td>
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<td>1.25</td>
<td>1.246</td>
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<td>4.5324</td>
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### Table 14: Thickness Correction Factor (after ref. 1)

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<tr>
<th>$t/s$</th>
<th>$C_{F_t}$</th>
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### Table 15: 4 point probe current settings (after ref. 3)

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<tr>
<th>Approximate Resistivity (Ω-cm)</th>
<th>Set Current for (mA)</th>
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<td>0.012</td>
<td>100</td>
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<td>40 - 1200</td>
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**References**


One of the most mundane operations performed in silicon integrated circuit processing is wafer cleaning. It is also one of the most important and difficult steps to perform well. There are three broad categories of contamination that must be removed by the cleaning process: organic residue (photoresist, organic solvent residues, synthetic waxes, fatty acids from human contact); inorganic ions (sodium, potassium, calcium); and inorganic atoms (gold, copper, iron). The following cleaning process is an adaptation of the so-called "RCA Clean", named after the work done by Kern and Puotinen at RCA Laboratories in 1970.

1. Gross organic contamination removal:
   (note: depending on the level of the contamination certain of the steps below may be omitted).
   a) Immersion in hot trichloroethane (TCA) in ultrasonic bath.
   b) Immersion in hot acetone in ultrasonic bath.
   c) Immersion in ethanol.
   d) High purity water (HPH2O) rinse.

   This sequence is our standard quick organic strip. Each subsequent rinse is a solvent for the one immediately preceding it. The idea is to finish with a very high purity, non-volatile solvent (i.e. the HPH2O). This can be blown off the wafer. It is important to never allow a cleaning solvent to evaporate directly from the surface of the wafer; if it does any impurities will simply remain behind on the silicon.

2. High purity organic strips:
   (note: these two steps may be used in sequence, or separately)
   a) Oxygen plasma strip: The O2 plasma is a very efficient way of "burning" off organics (see OP-K). This process, if used for a sufficient time, will remove almost any organic contamination. It may, however, also damage any metal present that is susceptible to oxidation.
   b) Caro's Acid (Pirana etch): immersion in a 1:1 solution of concentrated H2SO4 and 30% H2O2. **This is a very vigorous oxidizing solution**, and is commonly used in industry. Bath temperature is typically 95° C, immersion for about 15 min. Finish with HPH2O rinse.

3. Trace organic strip (RCA solution 1):
   a) Immersion in SC-1 solution, consisting of 5:1:1 to 7:2:1 parts H2O : H2O2 : NH4OH (30% H2O2, 27% NH4OH). All of the preceding organic strips will leave a trace organic film; this is the only process that has been found to be highly effective in removing this final
contamination layer. Typical bath temperature is 75 - 85°C, immersion time 10-20 min. Care must be exercised since NH4OH will etch bare silicon. In the presence of H2O2 a thin layer of SiO2 is formed which protects the silicon; if insufficient H2O2 is used, or the bath is old (the H2O2 breaks down to H2O and O in about 40 min) etching will occur. Finish with HPH2O rinse.

b) Removal of the SiO2 layer formed by SC-1 solution: etch in dilute HF, about 60 sec; finish with HPH2O rinse.

4. Inorganic contamination removal (RCA solution 2):
   a) immersion in SC-2 solution, consisting of 5:1:1 to 7:2:1 parts H2O : H2O2 : HCl (30% H2O2, 37% HCl). This solution has been found to be highly effective in removing almost all metallic contaminates through acid complexing reactions. Typical bath temperature is 75 - 85°C, immersion time 20 min. Finish with HPH2O rinse.

One final note: in our lab we do not follow these cleaning procedures rigidly, mainly for convenience sake. One particular problem is the glassware necessary for very high purity work: the pyrex used in our common beakers is a source of both sodium and boron, which can recontaminate the cleaned wafers. In industry only pure quartz would normally be used for the etching and cleaning tanks.

References


Plasma "ashing" is a very effective technique used to remove trace organic contamination from the surface of a chip. This is accomplished by using a RF plasma discharge to create highly reactive oxygen species (excited molecular O$_2$, ionized O$_2$, ionized atomic oxygen, and some excited ozone, O$_3$) which combine with the organic compounds. The resultant products are mostly the volatile species H$_2$O, CO$_2$, and CO. This process of "burning" organic material is one of the oldest uses of plasma processing in the semiconductor industry.

Our plasma asher is a particularly simple example of a barrel reactor. A pyrex cylinder is used for the vacuum chamber, and is surrounded by the RF electrode plates. A 13.56 MHz power source drives the plates, creating a plasma inside the chamber. In our unit we use a needle valve to regulate the flow of O$_2$ into the reactor so that a pressure of approximately 0.5 Torr is maintained. Between 50 and 100 watts can be delivered to the plasma.
Front Panel, Figure 1: Reference Numbers from Left to Right in Figure 1.

1. AC Power On/Off Button:
   Button is lighted when "ON".

2. Vacuum Toggle Switch:
   Controls both solenoid valves (vacuum and atmosphere);
   in down position reaction chamber is open to
   atmosphere and closed to vacuum pump. In "up"
   position chamber is open to vacuum pump and closed to
   atmosphere.

3. RF Power Toggle Switch:
   "Up" Position RF power is applied to electrodes;
   "Down" position RF power is "Off".

4. Level Knob:
   Adjusts RF power level 0-100 watts.

5. Tuning Knob:
   Adjusts variable capacitor to tune circuit (indicated
   by dip in meter reading).
Operating Procedure

1. The Plasmod should be on (AC power) when you arrive. If it is not, turn both it and the vacuum pump ON, and allow 10 minutes for warm-up.

2. Make sure both the VACUUM and RF POWER switches (see fig. 1) are OFF, then open the door and carefully slide out the pyrex tunnel. There should be a large petri dish or a slotted wafer boat inside. These are NOT ATTACHED TO THE TUNNEL, SO BE CAREFUL.
Set the tunnel on the table, open end facing you.

3. Set your samples on the petri dish, side-to-be-cleaned up, or in the wafer boat.

4. Close door and turn vacuum switch on. Watch pressure gauge; it should pump down to about 100 mTorr in 30-60 sec.

5. Turn O₂ Supply ON; use only the toggle value on the gas panel. DO NOT ADJUST NEEDLE VALVES.
The pressure should rise to about 600 mTorr.

6. Make sure RF POWER LEVEL knob is set to minimum (fully ccw). Turn RF power switch ON, then turn POWER LEVEL KNOB cw until the power meter reads approx. 50 W.

7. Immediately adjust the RF TUNING KNOB until the RF POWER METER registers a minimum (tune for a dip). A glow discharge should appear in the chamber as a pale purple glow.

NOTE: IF NO DISCHARGE APPEARS AND YOU CANNOT GET THE POWER METER TO REGISTER A MINIMUM, IMMEDIATELY TURN THE POWER LEVEL DOWN, AND THE RF SWITCH OFF.
ASK FOR ASSISTANCE.

8. Once the discharge appears, increase the power level to maximum (fully cw), and re-tune, again for a minimum. Continue to monitor tuning and discharge throughout the ashing cycle.

9. Ashing time depends on how serious the contamination is. Approximately 5 min. is usually adequate.

SHUT DOWN
10. Turn power level to minimum (fully ccw). Turn RF POWER switch OFF.

11. Turn O₂ supply OFF, THEN turn VACUUM/VENT switch OFF (down). This will disconnect the vacuum pump from the chamber and also vent the chamber to atmosphere.

12. Open door, carefully remove the tunnel and your sample, then replace the tunnel. NOTE: THE CHAMBER, PETRI DISH, AND SAMPLE WILL BE QUITE HOT!

DO NOT TURN THE AC POWER OFF. LEAVE PLASMOD ON UNTIL THE END OF THE LAB PERIOD.

End of Lab Shut-down:

1. Turn vacuum pump OFF.

2. With Plasmod still ON, slide the tunnel out slightly, and then turn the Vacuum Toggle Switch ON (i.e. up). This will vent the rough pump to atmosphere, which MUST BE DONE whenever the pump is switched off.
The fabrication of planar semiconductor devices and integrated circuits requires the formation of patterns on the surface of the circuit substrate. The process most commonly used to form these patterns is called photolithography. This technique uses a thin, photosensitive organic film, called photoresist, to transfer the pattern from a master mask to the IC substrate. Figure 34 illustrates the photolithographic process for two basic kinds of resist material, positive photoresist and negative photoresist. In this example the ultimate objective of the process step is the formation of openings to the silicon surface through a SiO$_2$ film, which could then serve as either a diffusion mask or a contact pattern. To begin the process the wafer is cleaned and dried, and the photoresist (PR) is applied. The PR is supplied in a viscous liquid form; it can easily be formed into a very thin (about 1 $\mu$m) and uniform layer by spinning a liquid-coated substrate at high speed. During the spin most of the solvents in the resist evaporate, but after spinning a pre-bake is performed to further dry and harden the film. As shown in the top segment of Fig. 1, the resist is exposed through a mask with the desired pattern on it. For a negative PR, the exposed areas are rendered insoluble by exposure to light. When immersed in a developer solution the unexposed regions are dissolved, leaving exposed regions covered by the resist. For a positive PR, the exposed regions are rendered soluble by exposure to light, and so after development only areas unexposed are still covered by resist. The resulting patterned substrate must then be placed in an etch (in this example, buffered HF), for which the resist serves as an etch mask. In this OP we are concerned with the application and development of the photoresist.

We use exclusively positive photoresists in our laboratory. There are a number of reasons for this, several of which will be discussed in lecture. Two important reasons are the somewhat simpler developing process (a slightly alkaline solution followed by a water rinse) and more durable film produced by positive resist. The characteristics of the resist we use are given in the data sheet on page IV-3.

Note that for these resists any area exposed to light will wash off in the developer, so care must be taken to avoid accidental exposure. Our Litho Room has yellow lights which do not expose the PR; the regular fluorescent room lights, as well as an unfiltered microscope illuminator, will expose the PR. Be careful not to expose a chip to these lights until it has been exposed with the mask aligner and developed.
Figure 34: Basic lithographic process (adapted from Introduction to Microlithography, Thompson et al)
The operating procedure for processing the positive resist we use is given on the next page. Several important features should be noted:

- Pre-bake: dries and hardens film; time, temperature, humidity affect photospeed of resist
- Exposure: check Mask Aligner log book for current time
- Development: there is a large development latitude so time is not critical; make sure to fully rinse chips HPH₂O before drying
- Flood Exposure: required to make removal of post-baked resist easier; during exposure positive PR liberates N₂, which if the exposure intensity is too high, can cause resist lift-off from substrate; this is the reason for the 5 sec/pause/5 sec/etc exposure used here
- Post-bake: required to harden PR and to improve adhesion of PR to substrate for later wet etch steps

References


Operating Procedure OP-L

1. Dehydration bake: Bake out the sample in the Post-bake oven for 5 mins. (The Post-bake oven is set at a temperature 125˚C).

2. Place chip on spinner chuck. Carefully open the Adhesion Promoter bottle and using the eyedropper, put a drop or two of Adhesion promoter at approximately the center of the sample. (When replacing the dropper, DO NOT spill any Adhesion fluid onto the threads of the bottle top.) Start the spinner (step on foot pedal). If necessary, adjust controller for spin rate of approximately 4000 rpm. Set timer for 30 sec.

3. Apply Photoresist: At the end of spin-cycle, repeat Step 2 using the positive photoresist (AZ1350J or equivalent). We are using a syringe-like dispenser with a particulate filter to remove any large "boulders" that could contaminate your film. See TA's for instructions on proper use of these dispensers. Don't be afraid to use too much photoresist, since the excess will spin off.

4. Pre-bake: At the end of the spin cycle, remove the sample and do a 10 min pre-bake in the pre-bake oven at 95˚C.

5. Expose: The sample is now ready for alignment and exposure: use OP-O, align the sample with the appropriate Mask on the Micro-Tech Mask Aligner. Having aligned the sample with the Mask, do a 15 sec. exposure to UV light. CHECK FOR NEW EXPOSURE TIME IN LOG BOOK. At the end of the exposure, remove the sample, replace the mask in the appropriate container. The sample is now ready for development.

6. Develop: The development station is located on the left side of the sink. The station has 3 beakers marked Developer, H2O, and H2O. (The three beakers should be set up by the T.A.). Using a pair of tweezers, dip the sample into the developer for 60 sec. Remove the sample at the end of the 60 sec. and rinse in the water in the next two beakers. Carefully blow sample dry. Inspect.
7. Flood expose under UV lamp for approx. 5 sec., pause, 5 sec., pause, 5 sec., for a total of 15 sec.

8. Post Bake: in the post bake oven, perform bake at 125°C for 10 min. The sample is now ready for any subsequent processing.

Resist Developer make-up:

18. AZ Developer: high purity water, in ratio 1:1.
19. Approximately 80-100 ml will develop about 4 chips.

Basic Photolithography

1) CLEAN YOUR SUBSTRATE!!!!
   Photoresist does NOT like to stick to DIRTY or WET substrates.
   Immediately prior to PR application a dehydration bake is a good idea: 125o, approx 5-10 min.

2) SPIN ON PHOTORESIST
   Make absolutely sure your sample COMPLETELY COVERS THE VACUUM CHUCK. First apply adhesion promoter (a couple of drops) and spin dry (check the spin speed during this step). Now apply a few drops of photoresist in the center of the chip. Spin: 4,000 to 5,000 rpm, 30 sec.

3) PREBAKE: 95°C, 10 min.; the time is important.

4) EXPOSE: note: the UV lamps take approx. 15 min to warm up.

   Turn the aligners OFF when you finish. DO NOT TURN OFF THE UV LAMP unless everyone is done for the day. THE LAMPS MUST COOL 30 min. AFTER THEY ARE TURNED OFF BEFORE THEY CAN BE RESTARTED.

5) DEVELOP:
   AZ Microposit Developer, diluted 1:1 with DI water.
   Time: normal process: approx. 60 sec.
DEVELOPER SHOULD BE USED ONLY IN BEAKERS LABELED FOR IT. NEVER PUT DEVELOPER IN BEAKERS LABELED FOR WATER. After use dispose of developer in sink; don't be stingy in how much you use—developer is cheap. RINSE ALL BEAKERS THOROUGHLY AFTER USE.

6) RINSE thoroughly in DI, blow dry.

7) FLOOD EXPOSE: approx. 5 sec., pause, 5 sec.

8) POST BAKE: 125°C, 30 min.
OP-M: Introduction to Capacitance Measurements

This section is intended as a brief review of semiconductor device physics as they pertain to capacitance-voltage measurements on the devices made in our lab. For more detailed information see, for example, Streetman's *Solid State Electronic Devices* (Prentice Hall, 1980) and Nicollian and Brews' *MOS Physics and Technology* (Wiley, 1982).

**NOTE:** All capacitance measurements are affected by the fact that any real device has finite "leakage current". From a circuit perspective, the real device under test is at best a parallel C - G circuit (i.e., a capacitor in parallel with a conductance G). To interpret measured data it is critical that you either know or can estimate whether the device is dominated by current flowing through the capacitor, or the conductance, or is split between the two with significant contribution from each. For a frequency independent capacitance and conductance, which dominates is clearly frequency dependent since the capacitive admittance has magnitude of \( \omega C \). Hence, for a device dominated by the capacitance, the inequality \( G / (\omega C) \ll 1 \) should hold. If the measuring instrument used determines the complex admittance at a given frequency, then you should be able to calculate this ratio; to apply the C-V analysis discussed below you must have \( G / (\omega C) \ll 1! \)

### A. p-n Junction Diodes

Due to the differences in Fermi level position relative to the band edges for p-type and n-type semiconductors, at a p-n junction in thermal equilibrium (or under reverse or small forward bias) there exists an electric field across a transition region of width \( W \) that straddles the metallurgical boundary. Within this "depletion" region the field sweeps out all free carriers, leaving behind uncovered (exposed) donor and acceptor ions. See Figure 35 for an abrupt junction under zero bias.

**Figure 35: p-n junction capacitance**
When a small ac voltage is applied on top of a dc reverse bias (which determines $W$) the width of the transition region varies as fewer or more impurity charges are uncovered at the edges of the region. This variation gives rise to a junction transition capacitance:

$$C = \frac{dQ}{dV} = \varepsilon_s \varepsilon_0 A / W$$  \hspace{1cm} (1)

where $\varepsilon_s$ is the dielectric constant of the semiconductor, $\varepsilon_0$ is the permittivity of free space, and $A$ is the junction cross-sectional area.

The thickness of the depletion layer $W$ will depend on the doping profiles on both sides of the junction, as well as the magnitude and sign of any applied bias. For increasing reverse bias the depletion width increases, so the transition capacitance decreases. Under small forward bias $W$ becomes very small, and the transition capacitance reaches a maximum. In general, the relation between junction capacitance (per unit area) $C'$, applied voltage $V_a$, and doping profiles $N(x_n)$ in the n-type material and $N(x_p)$ in the p-type, is quite complex:

$$N(x_n) = -\left( \frac{C'}{\varepsilon_s \varepsilon_0 q} \frac{dC'}{dV_a} \right) \left[ 1 + \frac{N(x_n) / |N(-x_p)|}{|N(-x_p)|} \right]$$  \hspace{1cm} (2)

where $x_n$ is the width of the depletion layer on the n-type side of the junction, and $x_p$ the width on the p-type side (so $x_n + x_p = W$). For an abrupt junction with one side much more heavily doped than the other, for example a $p^+-n$ junction, the term on the right side becomes one, and $N(x_n)$ can be determined by measuring the C-V curve of the diode. Also note that for such a diode $W \propto V^{1/2}$, so from eq. 1 we would expect $C \propto V^{-1/2}$. For a linearly graded junction $x_n = |x_p|$, $W \propto V^{1/3}$, and $C \propto V^{-1/3}$.

B. MOS Capacitors

A typical (non-ideal) C-V curve for a metal-oxide-semiconductor capacitor is shown below at both high and low frequency.

![Figure 36](image-url)
Here $C_O$ is the capacitance per unit area due to the oxide:

$$C_O = \varepsilon_0\varepsilon_{ox}/t$$

where $t$ is the thickness of the oxide. $C_T$ is the series combination of the oxide capacitance and the capacitance due to the depletion layer formed under the oxide:

$$1/C_T = 1/C_O + 1/C_S$$

where $C_S$ is the capacitance per unit area of the depletion layer $W_{max}$ deep

$$C_S = \varepsilon_0\varepsilon_{s}/W_{max} ; \varepsilon_S \text{ for silicon } = 12.$$  

For an n-type substrate (p-channel) the threshold voltage $V_T$ is given by:

$$V_T = (\phi_{ms} - 2\phi_F)/q - (Q_{SS} + Q_b)/C_O$$

where:

$$\phi_{ms} = \phi_m - (\chi_S + E_g/2 - \phi_F) \text{ n-type substrate}$$

$$\phi_F = (kT/q)\ln(N_b/n_i), \ N_b = \text{substrate doping level}$$

$$Q_b = qN_bW_{max}$$

$Q_{SS} = \text{total lumped excess surface states charge density}$

$$\phi_m = 4.25eV \text{ for aluminum}$$

$$\chi_S = 4.02eV \text{ for silicon}$$

$$E_g = 1.1eV \text{ for silicon}$$

$$n_i = 1.5x10^{10}\text{cm}^{-3} \text{ at room temperature for silicon}$$

Note that by measuring the C-V curves for our MOS capacitors we can obtain the threshold voltage, and from this estimate the total excess charge density in our oxides. This is process dependent, so this measurement is an important way of evaluating the quality of our grown oxides.
Capacitance-voltage measurements in our laboratory are done on a Materials Development Corp. MDC CBAX unit (see p.M-7 for machine control lay-out). The unit consists of:

1) a Boonton 72A Capacitance Meter
2) a Hewlett-Packard 7035B x-y plotter
3) a MDC C-V interface and ramp generator.

The C-V meter supplies a 15mV RMS capacitance measuring signal at 1MHz, while the interface unit ramp generator provides the following dc bias capabilities:

1) maximum + 150 V bias, adjustable via a ten-turn potentiometer
2) sweep over voltage range set above, at a rate that is adjustable from 0.1V/sec to 10V/sec via a ten-turn potentiometer
3) bias can be sweep from + to -, - to +, or held at any value in the sweep range.

Power-up Procedure and Initial Set-up

1. Turn the AC power switch on the Boonton meter ON; this will also power up the MDC bias supply.

2. Set the front panel controls as follows:
   a) Function: Zero
   b) Sweep Vernier: 10.0
   c) Positive Limit Vernier: fully counter-clockwise (i.e. zero)
   d) Negative Limit Vernier: fully counter-clockwise (i.e. zero)
   e) Sweep: 1 V/sec
   f) Meter Range Switch: 15 V
   g) Right side switches:
      i) Calibrate/Operate: calibrate
      ii) C-V/N-W: C-V

3. On the x-y plotter:
   a) select Pen-Up
   b) AC Power on
   c) set x & y sensitivities to 0.1 V/in
   d) insert graph paper, turn Chart Hold on
   e) turn Servo on
4. Zero the Capacitance Meter:
   With the sample on the probe station and all cables connected, place the probe tip just above the surface of the device to be tested. Select the 3pF range on the Boonton, and use the Zero Control to set the meter to zero.

5. Set Capacitance Meter range to 3000pF; carefully lower probe tip onto sample.

6. Set desired + and - limits:
   a) set Function switch to appropriate Set (either +set or -set)
   b) slowly turn the Limit vernier to increase the bias to the desired maximum value (usual in the 10 to 15 V range for MOS capacitor and diode measurements)
   c) re-adjust Capacitance Meter range as necessary.

7. Adjust x-y plotter range to allow full C-V curve to fit graph paper.

8. For sweep from Negative Limit to Positive Limit: select +SWEEP Function.
   For sweep from Positive Limit to Negative Limit: select -SWEEP Function.

9. When C-V measurements are completed, set Function to ZERO before raising probe tip from device under test!

10. Power off system when done.

PCASP CV
    M-7
The determination of junction depth is an important aspect of semiconductor process evaluation. In our lab the junction is a result of the pre-dep and drive-in processes performed at high temperature. Although there are a variety of models that can be used to estimate the distance over which the impurities diffuse, and thus determine junction depth, there are also many severe assumptions that must be made to apply the models. It is always desirable to actually measure the junction depths; however, when considering that the distances to be measured are only about a micron, and that impurity concentrations to be sensed are perhaps only $10^{-8}$ of the semiconductor atomic density, such measurement presents a non-trivial challenge.

Fortunately, there is a relatively simple technique for junction depth measurement which makes use of a mechanical grinding process combined with differential chemical staining. The objective of the grinding process is to convert very shallow depth information into large lateral variations. Figure 1 below illustrates the geometrical advantage of grinding a groove into the surface of our doped chip. $W_2$ and $W_1$ are measured with a microscope (see OP-S, p. 183 for line width measurements).

![Figure 37: Junction sectioning geometry.](image)

Because of the large radius of the grinding tool, the lateral dimensions which are exposed are quite large. If a chemical stain (consisting of metal salts in an electrolyte) is applied
to the exposed p-n junction, and then exposed to light, a preferential staining of the n-type regions will occur. An optical microscope (see OP-S p. 183 for instructions on the use of our line width measuring equipment) can then be used to measure the two dimensions $W_1$ and $W_2$. Applying some geometry yields the relationship:

$$x_j = d_2 - d_1 = \sqrt{R^2 - \left(\frac{W_2}{2}\right)^2} - \sqrt{R^2 - \left(\frac{W_1}{2}\right)^2}$$

At present we use a PHILTEC 2015 Sectioner, with a tool radius $R$ of 19,050 µm. In addition, Philtec has determined that a slight correction factor is necessary to match the results with ASTM standards. Thus, the formula used to determine junction depth is given by:

$$x_j \text{ (µm)} = \sqrt{(19,050 \text{ µm})^2 - \left(\frac{W_2 \text{ (µm)}}{2} - 9.924\right)^2} - \sqrt{(19,050 \text{ µm})^2 - \left(\frac{W_1 \text{ (µm)}}{2} - 9.924\right)^2}$$

Operating Procedure

The basic operation of the Philtec Sectioner is quite simple. The main parameter that must be determined in our application is the sectioning time (see step 8 below). This time is dependent mainly on the type of diamond grinding paste used to dress the spindle (see section 4 below). The operating procedure given on the next pages is a copy of the Philtec instruction sheet. We will give an update on operation in the lab during which you actually perform the junction grooving.

As of Aug. 25, 1988 the following parameters produced acceptable results:

Sectioning time: 10 sec
Staining time: 10 sec
Illumination source: Stereozoom 7 scope, 5X, illuminator power supply setting 3
OP-O: Mask Alignment and the Microtech Mask Aligners

filename: MCROTCH

In order to fabricate IC devices it is necessary to accurately align patterns already present on a chip to the next pattern in the lithography sequence. The instrument used for this purpose is called a Mask Aligner, for the obvious reason that it aligns a mask to a pattern already on the chip; it also exposes this pattern in the photoresist after the alignment is complete. We use a manual alignment procedure, which is probably the most challenging and time-consuming step in our lab processing. The purpose of this OP is to familiarize you with the operation of our Microtech Mask Aligners, and to provide some tips on how to perform your alignments. Fortunately, we have upgraded these aligners significantly, and you should now find them somewhat easier to use.

A mask aligner must serve two purposes: first, it must provide a means to align a pattern on a chip to the pattern on a mask; and second, it must then expose this pattern. Our aligners use a rigid frame which holds the mask that moves (ideally) only in the vertical direction (z-axis), and a separate wafer chuck which holds the chip that can rotate about the z-axis (θ axis) and move in the horizontal plane (x-y plane). A very small gap is set between the chip and mask, and a microscope is used to examine the mask pattern and alignment marks on the chip simultaneously. The x-y and θ adjustments are then used to bring the two patterns into alignment. After alignment, the mask and chip are pressed together by using a vacuum to apply about 14 pounds per square inch of pressure to them. A timer is used to open a shutter, allowing a UV lamp to expose the photoresist.

The most difficult step in this process is the alignment of chip to mask. In industry special alignment marks and automated pattern recognition are used to perform this step. We must perform the process manually, however. The technique that will allow you to achieve precise alignment in a relatively short time is called split-field alignment. The mask aligner microscope actually has two objective lenses, side-by-side. When in the split-field mode, the image you see is split in half, with the left image corresponding to one location on the chip, and the right half corresponding to another location about one inch away. By adjusting the separation of the objective lenses you will be able to see the same type of alignment marks at two widely separated points on the chip. When the θ and x-y translators are used to move the chip it will be very easy to tell when the whole chip is aligned, since you can see both of these areas. With this technique we can achieve alignment tolerances of better than ±5 μm, which is adequate for our minimum critical dimension of about 20 μm.

Tips on Using the Microtech Mask Aligners

One of the most important factors in aligning is maintaining the smallest possible separation between mask and substrate during alignment. With these aligners the best technique is to initially place the mask and chip in hard vacuum contact. You should then focus the microscope on the chip and mask patterns. While watching through the
microscope, slowly pull out the z-axis separation lever; as the mask rises away from the chip it will go slightly out of focus. You should then use the x-y translation micrometers to check for adequate separation: if there is not enough gap to completely separate mask and chip, when you try to move the chip the mask will be dragged along with it, which is clearly visible through the microscope. There is no substitute for practice in this process, so be patient until you develop a feeling for how the machines operate.

Please be careful while using the mask aligners: it is relatively easy to scratch both masks and your chips if you use the aligners improperly.
Figure 38: Schematic diagram of the Microtech Mask Aligner
Mask Aligner Operating Procedure

1. Start the U.V. lamp:

   Turn the U.V. Lamp Power Supply on, and then depress the START BUTTON for approximately 1 sec. The lamp should start immediately. Allow a MINIMUM 15 MINUTE WARM-UP PERIOD.

   Step 1 should normally be performed by the Lab TA before you arrive.

2. Turn the Aligner ON. Pull the Contact/Separate Control Knob all the way OUT (full separation position between substrate and mask).

3. Load the Mask:
   a) Slide the Substrate Chuck all the way forward by pulling on the Substrate Chuck Slide Knob.
   b) Slide out the Mask-Holder Tray.
   c) Load mask, pattern side down.
   d) Slide Mask-Holder Tray back into the Mask Frame.

4. Load the Substrate:
   a) The Substrate Chuck should still be out from step 3a.
   b) Place your sample on the center of the chuck; orient it so it will be roughly aligned with the mask pattern.
   c) Turn the Substrate Vacuum ON.
   d) Slide the Substrate Chuck all the way back under the Mask Frame.

5. Check for Coarse Alignment:
   Check the rotational alignment visually; if necessary, slide chuck back out (step 3a) and rotate the chuck manually.

6. Planarize Substrate to Mask:
   a) Turn the Substrate Vacuum OFF.
   b) Slowly push the Contact/Separate Control Knob back in; the Mask Frame should drop down towards the substrate, rapidly at first, and then more gradually.
   c) When the Contact/Separate Control Knob is all the way in (full vacuum contact position) the substrate and mask should be in hard vacuum contact. Sample is now planarized.
d) Turn the Substrate Vacuum back ON.

7. Align:
   a) To move the chip relative to the mask the Contact/Separate Control Knob MUST be in the SEPARATE Position: from fully-in position (hard vacuum contact) slowly pull the knob toward you. The Mask Frame will rise slightly, allowing free motion of the Substrate stage. Watch for it through microscope, mask image will blur.
   b) Use the rotation micrometer to achieve \( \theta \)-axis alignment; check opposite corners of your chip with the microscope to determine \( \theta \)-axis.
   c) Use the Fine Translation Micrometers to align in x-y plane. Check several locations on the wafer with microscope.

USE OF SPLIT-FIELD ALIGNMENT:
Put microscope in split-field mode; the image seen through the microscope should now appear cut in half, the left side corresponds to the right microscope objective lens, and the right side of the image to the left objective. Locate an alignment mark in one field; turn the Objective Lens Separation Adjustment (located to the right of the two objective lenses) until both fields show the same alignment mark. It should now be possible to simultaneously perform \( \theta \) and x-y alignment.

d) Push the Contact/Separate Control Knob all the way in (hard contact position).

e) Check alignment again with microscope; if necessary repeat steps a-d. When alignment is satisfactory, make sure the Contact/Separate Control is in the contact position.

8. Expose:
   a) Pull the microscope head all the way forward to bring the mirror over the sample.
   b) Set timer for desired exposure time.
   c) Press Expose button.

9. Remove your sample:
   a) After the expose cycle is complete, pull Contact/Separate Control all the way out to the fully separated position.
   b) Slide the Substrate Chuck all the way out, turn the substrate vacuum off, and remove your sample.
10. Remove mask:
   a) The substrate chuck should still be out from step 9b.
   b) Slide out the Mask-Holder Tray. Carefully remove the mask, and replace it in its storage box.
   c) Slide the Mask-Holder Tray back in; slide the Substrate Chuck back in. Turn the Mask Aligner Power switch off.

   **DO NOT TURN THE UV LAMP POWER SUPPLY OFF.**
OP-P: Hydrofluoric Acid Etching

As discussed in the Safety section of the Lab Manual Introduction (p. 10), hydrofluoric (HF) acid can be very dangerous if mishandled. It is, however, a very useful etch for silicon dioxide, SiO₂. It has a number of advantages over other techniques when patterning SiO₂ over silicon: it has very high selectivity over silicon, i.e. the etch rate of SiO₂ in HF is much greater than the etch rate of Si; HF can easily be masked by photoresist; the etch rate is quite repeatable, and remains constant even after a large number of samples have been etched; and the equipment required to etch with HF is relatively simple and inexpensive.

The actual etchant we use is a solution of concentrated HF (49%), water, and a buffering salt, NH₄F, in about the ratio 1:6:4. This solution is referred to as buffered HF, or BHF. The buffering agent is added to maintain a constant pH as the HF is consumed in its reaction with SiO₂:

\[
4\text{HF} + \text{SiO}_2 \rightarrow \text{SiF}_4 + \text{H}_2\text{O}
\]

Since the etch rate is a function of the solution pH, BHF has a much more controlled etch rate (about 1000Å/min at room temperature) over the life of the etchant.

In order to safely handle our BHF etching a special etch station has been designed for our lab. Figure 39 shows a top view of our station, and Figure 1b shows the plumbing arrangement for the station.

![Figure 39: top view of BHF etch station.](image-url)
Our system consists of three dump-type rinse tanks installed in the work top of a fume hood. Each tank has a DI water supply, controlled by a water valve in front of the station. The tanks are made up of an inner cup to which the water is supplied; this cup fills until it overflows into the outer portion of the dump tank, which is connected to an acid drain. We use the first tank on the left for an introduction rinse to wet the samples to be etched; the middle tank holds a teflon etchant cup, which actually contains the BHF; the last tank on the right is used for a water rinse to remove the BHF.

In addition to the dump tanks we use a special splash guard to prevent accidental acid spills. This consists of a plexiglass cover with large openings above the two end rinse tanks. These openings are connected by a narrow slot which passes over the etch cup (see Fig. 1a). To begin an etch step, the substrates to be etched are placed in a teflon chip carrier with a long handle attached. This carrier is then lowered into DI water through the opening over the first rinse tank. After wetting the samples the carrier is raised and transferred to the etch cup. The slot in the splash guard is large enough to allow the handle to pass through, but is not large enough to allow the chip carrier to be removed. When the etch is finished, the carrier is raised clear of the etch cup, and is transferred to the final rinse tank. After a suitable rinse time the chip carrier can be removed through the large hole in the splash guard over this tank. We have found this system will prevent HF splashing in almost all circumstances.
BHF ETCH PROCEDURE

1. Place samples to be etched in the teflon carriers located on the bench to the left of the etch station. Make sure a long teflon handle is inserted into the carrier.

2. Turn on the water supply to the two end dump tanks; make sure the two regular water faucets are on and running into the sink.

3. Put on a pair of acid resistant gloves (the green gloves next to the hood) and a pair of protective eye glasses. DO NOT LEAVE THE HOOD AREA ONCE YOU START THIS PROCEDURE!

4. Carefully lower the sample carrier through the splash guard into the left-most rinse tank. Leave immersed for approximately 15 sec.

5. Lift the carrier out of the rinse water, and carefully shake off any excess water. Now slide the handle down the slot to position the wafer carrier over the BHF cup. Very carefully lower the carrier into the cup. Be sure not to splash any HF out of the cup.

6. Use the running water in the sink to thoroughly rinse your gloves. DO NOT REMOVE YOUR GLOVED HANDS FROM THE HOOD DURING THE ETCH TIME: REMAIN AT THE ETCH STATION UNTIL THE PROCESS IS COMPLETE.

7. At the end of the desired etch time carefully lift the carrier out of the etch cup, and gently shake any drops of BHF off the carrier back into the cup. Now transfer to and immerse the carrier in the right side rinse tank. RINSE FOR AT LEAST 1 MIN.

8. Use the HP H₂O dispenser to rinse the handle of the carrier, as well as your gloves. MAKE SURE ANY SURFACES THAT MAY HAVE BEEN CONTAMINATED WITH HF ARE RINSED IN WATER.
9. Remove the carrier from the rinse tank, and finish with at least two HP H₂O rinses in the teflon beaker in front of the etch station.

10. After completing the rinse remove the carrier from the hood, and transfer to the wafer spinner. Go back to the hood and thoroughly rinse your gloves in running water in the sink. Remove acid gloves, leaving them at the hood.

11. Remove your clean gloves, throw them away, and go to the large sink in the Litho Room for final wash up. Be careful to rinse your hands and arms thoroughly, especially under the fingernails.
OP-Q: Tektronix Curve Tracer

This section is intended as an introduction to the use of our Tektronix Curve Tracer. This is a very versatile instrument, capable of both two-and three-terminal measurements. Section I describes the operation of the curve tracer for two-terminal measurements (i.e. diode, capacitor, or resistor characteristics) and Section II for three-terminal measurements (bi-polar transistor or MOSFET characteristics).

Section I: Two-Terminal Devices

In this mode the device-under-test (DUT) is connected between the C and E terminals of the curve tracer. The Collector Supply section (see Figure 41) will then apply a voltage at the C terminal, Vc. Note the Max Peak Volts selector and its concentric knob, the Series Resistor selector. The Max Peak Volts selects the maximum voltage that can be applied to the DUT, while the Variable Collector % knob is a multiplier of this peak voltage, determining the actual max voltage applied. The Series Resistor selects the value of series resistance between the voltage source and the DUT, serving as a current limiter. The Collector Supply Polarity selector allows you to choose between a plus and minus Vc sweep, plus only sweep, minus only sweep, and DC applied voltage (either minus or plus) controlled by the Variable Collector % knob and the Max Peak Volts selector.

The display will now show the voltage across the C and E terminals (and therefore across the DUT) on its horizontal axis, scale set by the Horizontal section; and the current through the DUT on the vertical axis, scale set by the Vertical section. Also note directly above the Vertical current selector the Terminal Selector. This setting allows various Base and Emitter or Collector settings. We usually use the Emitter Grounded selections. For the Base setting, see section II.

Warnings:

1) Always make sure the Variable Collector % knob is set at 0% before making any electrical connections, or changing the Max Peak Volts or Series Resistor.

2) Normally start with Max Peak Volts set low (25 Volts) and the Series Resistor set high (> 10K). After making electrical connections, slowly increase the Variable Collector % setting until you obtain a curve trace. Then, if necessary increase Max Peak Volts and reset the Series Resistor.
3) When measuring reverse characteristics of diodes, the large diode capacitance may make the curve trace appear as a loop. To make accurate measurements, switch Collector Supply Polarity to appropriate DC setting, and sweep the trace manually at a slow rate. You can use the storage scope settings to record the trace.

4) The curve tracer can produce HAZARDOUS HIGH VOLTAGES. You will normally only need large voltages for diode breakdown measurements, but these may well be greater than 100 Volts. BE VERY CAREFUL NOT TO TOUCH ANY OF THE PROBES OR THE INSULATED SUBSTRATE CHUCK WHEN HIGH VOLTAGES ARE APPLIED.

Section II: Three-Terminal Devices

The display and E and C controls behave in an identical way to that described in Section I, but we now have an additional variable, the Base setting. This curve tracer can either inject current (for bipolar measurements) or apply voltage (for FET measurements), and can step this parameter from its maximum value to lower values in fixed steps, in order to produce the whole family of curves characterizing the DUT. The following is a description of the Step Generator section which controls the base parameter:

Step Family: determines whether only one value of the base term is generated, or whether multiple terms are.

Step Rate: sets rate at which base term is stepped.

Polarity: sets the step voltage polarity of base term relative to ground; for the voltage mode, applies same polarity as collector sweep volts relative to ground in Normal mode, opposite in Invert mode.

Step/Offset Ampl: determines whether current or voltage is applied to B terminal. In conjunction with the Offset Multi control, sets the maximum current/voltage applied. Also sets the size of the steps used for changing the B parameter when Step Family is set to Rep position.

Note: the X.1 button decreases the step size by a factor of 10, BUT DOES NOT DECREASE THE MAX BASE PARAMETER: see Offset Multi.

Number of Steps: sets number of steps applied to B parameter.
Offset Multi: multiplies (0 to 10x) normal step amplitude set by step/offset Ampl. control to determine the starting value of the base parameter. Note this value is set by multiplying the Offset Multi setting by the normal (i.e., the value the dial pointer indicates, regardless of whether the X.1 button is depressed) Step/Offset Ampl setting. Also note this dial is a vernier tenturn indicator, and reads to three significant figures.

Measuring Procedure for MOSFETs

Normal circuit configuration:

<table>
<thead>
<tr>
<th>Drain</th>
<th>Collector</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
<td>Emitter</td>
</tr>
<tr>
<td>Source</td>
<td>Base</td>
</tr>
</tbody>
</table>

DUT    Curve Tracer

p-channel (n-type substrate):

The following Collector Settings allow us to apply a voltage VDS of up to negative 25 Volts to the drain:

Variable Collector: 0%
Max Peak Volts: 25
Series Resistor: 2 k
Collector Supply Polarity to -

Now we must set up to apply negative gate voltages from the Step/Offset amplifier:

Step/Offset Ampli: 1V, Step X.1 button out (i.e. on)
Step Family: Rep on (in)
Step Rate: Norm on (in)
Step/Offset Polarity: inverted (out)
(this adds positive gate bias steps to the starting value set by the Offset Multi dial)

Number of Steps: 1 (fully counter-clockwise)

Offset Multi: 0
Zero button below Offset Multi: offset (out)
Aid button: oppose (out)

These settings allow us to apply a series of negative gate voltages for the drain-source IV curves. The first gate voltage is fixed by the offset multiplier setting times the normal step/offset amplitude: i.e., (0 to 10) x 1 Volt, where we have initially set the multiplier dial to zero (0). The gate voltage steps are added to this max in steps of +0.1 volt (since the X.1 button is active). We have initially set the number of steps to one.

We now would adjust the horizontal and vertical scales, along with the position of the zero-zero dot, to obtain the desired display:

Horizontal Collector Volts: 1 V/div
Filter: normal (in)
Mag buttons on horizontal and vertical positions: off (in)
Vertical Collector current: 0.1mA/div
Terminal Selector: Emitter grounded, Step generator

With the offset multiplier set to zero, for an enhancement mode MOSFET, as the collector voltage % is increased no current should flow. Set this control for approximately 5 V collector voltage. Now SLOWLY increase the offset multiplier to apply a negative voltage (negative because the collector supply polarity is -)to the gate; when the threshold voltage is reached the MOSFET will turn on, and current will flow. Once the maximum current desired is reached by continuing to increase the offset multiplier, increase the number of steps control to obtain the complete family of curves.

n-Channel Settings:

For an enhancement mode n-channel device we need to apply positive voltage to the drain, and a positive gate bias to turn the device on:
The following Collector Settings allow us to apply a voltage VDS of up to positive 25 Volts to the drain:

Variable Collector: 0%
Max Peak Volts: 25
Series Resistor: 2 k
Collector Supply Polarity to +

Now we must set up to apply positive gate voltages from the Step/Offset amplifier:

Step/Offset Ampli: 1V, Step X.1 button out (i.e. on)
Step Family: Rep on (in)
Step Rate: Norm on (in)
Step/Offset Polarity: inverted (out)
   (this adds negative gate bias steps to the starting value set by the Offset Multi dial)
Number of Steps: 1 (fully counter-clockwise)
Offset Multi: 0
Zero button below Offset Multi: offset (out)
Aid button: oppose (out)

These settings allow us to apply a series of positive gate voltages for the drain-source IV curves. The first gate voltage is fixed by the offset multiplier setting times the normal step/offset amplitude: i.e., (0 to 10) x 1 Volt, where we have initially set the multiplier dial to zero (0). The gate voltage steps are added from this max in steps of -0.1 V (since the X.1 button is active). We have initially set the number of steps to one.

We now would adjust the horizontal and vertical scales, along with the position of the zero-zero dot, to obtain the desired display:

Horizontal Collector Volts: 1 V/div
Filter: normal (in)
Mag buttons on horizontal and vertical positions: off (in)
Vertical Collector current: 0.1mA/div
Terminal Selector: Emitter grounded, Step generator
With the offset multiplier set to zero, for an enhancement mode MOSFET, as the collector voltage \% is increased no current should flow. Set this control for approximately 5 V collector voltage. Now SLOWLY increase the offset multiplier to apply a positive voltage (positive because the collector supply polarity is +) to the gate; when the threshold voltage is reached the MOSFET will turn on, and current will flow. Once the maximum current desired is reached by continuing to increase the offset multiplier, increase the number of steps control to obtain the complete family of curves.
Figure 41: Front panel of Tektronix 577 Curve Tracer
Table 16: FUNCTIONS OF CONTROLS AND CONNECTORS for Tektronix Model 577 Curve Tracer

<table>
<thead>
<tr>
<th>Display Units</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>INTENSITY</td>
<td>Controls non-stored display brightness.</td>
</tr>
<tr>
<td>FOCUS</td>
<td>Provides adjustment to obtain a well-defined display.</td>
</tr>
<tr>
<td>POWER</td>
<td>Used to turn instrument power on and off.</td>
</tr>
<tr>
<td>BEAM FINDER</td>
<td>Brings beam on-screen; limits display to the area inside the graticule.</td>
</tr>
<tr>
<td>TRACE ROTATION (rear panel)</td>
<td>Permits alignment of the trace to the horizontal graticule lines.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DI Only (Storage)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>UPPER and LOWER STORE</td>
<td>Selects storage or non-storage operation.</td>
</tr>
<tr>
<td>UPPER and LOWER ERASE</td>
<td>Complementary cancelling switches select the screen to be erased. Both buttons pushed selects both screens.</td>
</tr>
<tr>
<td>BRIGHTNESS</td>
<td>Provides continuously variable flood-gun current duty cycle from about 10% to 100% (when the collector sweep is turned down or disabled), permitting extended retention of displayed information. Also controls the degree of spot dimming when the collector sweep is turned down or disabled.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Collector Sweep</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>COLLECTOR SUPPLY POLARITY (Automatic trace position with polarity change is maintained in all switch positions.)</td>
<td><strong>NOTE</strong>: The normal step generator polarity is positive-going in +DC, +, and AC, and negative going in - and -DC. Step generator polarity can be inverted by either the STEP/OFFSET POLARITY switch or the test fixture Terminal Selector switching.</td>
</tr>
<tr>
<td>+DC</td>
<td>Applies positive DC to the collector terminals of the test fixture. Useful when the device under test exhibits</td>
</tr>
<tr>
<td>Operation</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-------------</td>
</tr>
<tr>
<td>+</td>
<td>Applies positive sweeping voltage at 2X line rate to collector terminals of the test fixture. When the step generator is in PULSED mode, the supply is automatically switched to DC unless the operator desires to maintain the sweep voltage (see PULSED 300 µs).</td>
</tr>
<tr>
<td>AC</td>
<td>Applies AC at power line frequency to the test fixture collector terminals (use SLOW step rate).</td>
</tr>
<tr>
<td>-</td>
<td>Applies negative sweeping voltage at 2X line rate to the test fixture collector terminals. When the step generator is in PULSED mode, the supply is automatically switched to DC unless the operator desires to maintain the sweep voltage (see PULSED 300 µs).</td>
</tr>
<tr>
<td>-DC</td>
<td>Applies negative DC to the test fixture collector terminals. Useful when the device under test exhibits excessive looping in sweep mode, or when a DC supply is desired.</td>
</tr>
<tr>
<td>VARIABLE COLLECTOR %</td>
<td>Provides uncalibrated, continuously variable control of collector supply amplitude from 0% to 100% of the voltage selected with the MAX PEAK VOLTS switch.</td>
</tr>
<tr>
<td>MAX PEAK VOLTS Switch</td>
<td>Selects one of five collector supply voltages.</td>
</tr>
<tr>
<td>SERIES RESISTORS and PEAK POWER WATTS Switches</td>
<td>Fourteen resistor values coupled to the MAX PEAK VOLTS switch to maintain one of six labeled peak-power limits. The SERIES RESISTORS and PEAK POWER WATTS switch pulls out to unlock from the MAX PEAK VOLTS switch to change the power setting. Lower power settings are available on all except the highest voltage range.</td>
</tr>
<tr>
<td></td>
<td>The maximum peak power indicated by the MAX PEAK POWER WATTS can be delivered only if the</td>
</tr>
</tbody>
</table>
VARIABLE COLLECTOR % control is set to 100 and the impedance of the "device under test" exactly matches the series resistor selected with the SERIES RESISTORS switch.

The MAX PEAK POWER WATTS switch usually can be safely set above the maximum power rating of the device under test.

COLLECTORSUPPLY DISABLED (Indicator lamp) The yellow lamp is lighted when the test fixture protective lid is not closed over the test terminals (unless modified by a wiring option in the test fixture) whenever the MAX PEAK VOLTS switch is in the 100 V, 400 V, or 1600 V position. The yellow lamp pulses (on and off) if the vertical current limiting circuit disables the collector sweep (when the device under test current causes 2.5 times full-screen deflection for a short time).

COLLECTOR SUPPLY CIRCUIT BREAKER Protects the collector supply from excessive power dissipation. Push to reset breaker after circuit interruption.

<table>
<thead>
<tr>
<th>Step Generator</th>
</tr>
</thead>
<tbody>
<tr>
<td>PULSED 300 µs (Pushbutton) With the 300 us pushbutton in the in position (Pulsed mode), the step generator produces 300 us wide pulses at 1 or 2 times line frequency, depending on the Step Rate selected. For these two step rates (SLOW and NORM) the collector supply is automatically switched to DC unless the COLLECTOR SUPPLY POLARITY is in AC. If the FAST Step Rate is selected, the generator step rate is twice the line frequency, but the collector supply is not switched.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>STEP FAMILY</th>
</tr>
</thead>
<tbody>
<tr>
<td>REP With this pushbutton in the &quot;in&quot; position, up to ten steps per family are generated, depending on the position of the NUMBER OF STEPS control. When the push-push button, STEP X.1, concentric with the STEP OFFSET AMPL switch, is in the &quot;out&quot; position, the NUMBER OF STEPS control provides from about 1 to 95 steps.</td>
</tr>
</tbody>
</table>

| SINGLE Each time the SINGLE button is pressed, a single family |
is generated. Upon release, the step generator is turned off. Single family is useful for low-current, two terminal measurements.

<table>
<thead>
<tr>
<th><strong>SLOW (1X LINE Frequency)</strong></th>
<th>When the SLOW pushbutton is in the &quot;in&quot; position, the generator stepping rate is at power line frequency.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NORM (2X LINE Frequency)</strong></td>
<td>When the NORM pushbutton is in the &quot;in&quot; position, the generator stepping rate is twice the power line frequency.</td>
</tr>
<tr>
<td><strong>FAST (4X LINE Frequency)</strong></td>
<td>When the FAST pushbutton is in the &quot;in&quot; position, the generator stepping rate is four times the power line frequency.</td>
</tr>
</tbody>
</table>

**NOTE:** Step transitions occur at the start of the collector supply sweep in SLOW and NORM modes. Transitions occur at both the start and the peak of the collector supply sweep in the FAST mode.

<table>
<thead>
<tr>
<th><strong>FAST and SLOW</strong></th>
<th>When FAST and SLOW buttons are in the &quot;in&quot; position simultaneously, the generator stepping rate is twice the power line frequency, (NORM), but the step transitions occur at the peaks of the collector supply sweeps.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>NUMBER OF STEPS</strong></td>
<td>Continuously variable control selects the number of steps per display.</td>
</tr>
<tr>
<td><strong>STEP/OFFSET AMPL</strong></td>
<td>Selects from 21 current steps, from 50 nA/Step to 200 mA/Step, or six voltage steps, from .05 V/Step to 2 V/Step, in a 1-2-5 sequence.</td>
</tr>
<tr>
<td><strong>STEP X.1</strong></td>
<td>Push-push knob concentric with STEP/OFFSET AMPL knob. When this knob is released (&quot;out&quot; position), the Step Amplitude is reduced to .1X the previous amplitude and is indicated by the illuminated area of the STEP/OFFSET AMPL knob skirt. The OFFSET MULT range is not affected, resulting in small steps on large offset capability. The number of steps available changes (from the 1 to 10 range to approximately 1 to 95 steps), making the display appear as a ramp rather than discrete steps at the high rate.</td>
</tr>
</tbody>
</table>
| **STEP/OFFSET POLARITY** | When the NORM pushbutton is in the "in" position, the...
step voltage is the same polarity as the collector sweep unless inverted by the test fixture. When the NORM button is in the "out" position, the step voltage is opposite the collector sweep polarity unless inverted by the test fixture. The Offset polarity is determined by the position of the OFFSET/AID/OPPOSE button.

| OFFSET MULT | Multiturn control providing DC offset from 0 to 10 times the STEP/OFFSET AMPL switch setting with the STEP X.1 knob in the "in" position, or 0 to 100 times the STEP/OFFSET AMPL setting with the STEP X.1 knob in the "out" position. |
| OFFSET | In the "out" position, the offset voltage is determined by the OFFSET MULT control. When the ZERO button is in the in position, offset is disabled. |
| OPPOSE | In the "in" position, the offset voltage aids the step generator signal. When the OPPOSE button is in the "out" position, the offset voltage opposes the step generator signal. |

**Horizontal**

| HORIZ VOLTS/DIV(knob) | Selects from 12 calibrated collector deflection factors from .05 V/DIV to 200 V/DIV or from 6 calibrated base deflection factors from 50 mV/DIV to 2V/DIV with X10 HORIZ MAG PULL in the "in" position. With the X10 HORIZ MAG PULL in the "out" position, the deflection factors are 5 mV/DIV to 20 V/DIV or 5 mV/DIV to .2 V/DIV. All steps follow a 1-2-5 sequence. |
| Horis POSITION(knob) | Provides uncalibrated horizontal positioning over at least +10 graticule divisions. |
| X1O HORIZ MAG PULL | Pulling the Horiz POSITION knob to the "out" position provides ten times magnification of the horizontal display, extending the horizontal positioning to + 100 divisions. Sensitivity change is indicated by a change in the area of illumination of the HORIZ VOLTS/DIV knob skirt. |

**Display**
<table>
<thead>
<tr>
<th><strong>DISPLAY INVERT</strong></th>
<th>When the NORM pushbutton is in the &quot;in&quot; position, a normal display is presented. When the NORM button is in the out position, the display is inverted, both horizontally and vertically.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DISPLAY FILTER</strong></td>
<td>Full vertical bandwidth is obtained with the NORM pushbutton in the in position. When the NORM pushbutton is in the &quot;out&quot; position, vertical bandwidth is limited to reduce noise on the trace. Band-width limit is useful in the most sensitive CURRENT/DIV positions, DC positions of the collector sweep, and with base steps turned off. When sweeping manually with filter in use, sweep very slowly.</td>
</tr>
<tr>
<td><strong>Vertical</strong></td>
<td></td>
</tr>
<tr>
<td>Vertical POSITION(knob)</td>
<td>Provides uncalibrated vertical positioning over at least +-8 divisions.</td>
</tr>
<tr>
<td><strong>X1O VERT MAG PULL</strong></td>
<td>Pulling the Vert POSITION knob to the &quot;out&quot; position provides ten times magnification of the vertical display, extending the vertical positioning to +-80 divisions. Sensitivity change is indicated by a change in the area of illumination of the VERTICAL SENSITIVITY (Test Fixture) knob skirt.</td>
</tr>
<tr>
<td><strong>177 Test Fixture Terminal Selector</strong></td>
<td></td>
</tr>
<tr>
<td><strong>EMITTER GROUNDED</strong></td>
<td></td>
</tr>
<tr>
<td><strong>BASE TERM</strong></td>
<td></td>
</tr>
<tr>
<td><strong>STEP GEN</strong></td>
<td>Applies step generator output to the test fixture base connections.</td>
</tr>
<tr>
<td><strong>OPEN (OR EXT)</strong></td>
<td>Disconnects the test fixture base terminal from the step generator output and connects the base terminal to the front-panel EXT BASE OR EMIT INPUT connector.</td>
</tr>
<tr>
<td><strong>SHORT</strong></td>
<td>Disconnects the test fixture base terminal from the step generator output and grounds the base terminal.</td>
</tr>
<tr>
<td><strong>BASE GROUNDED</strong></td>
<td></td>
</tr>
<tr>
<td><strong>EMITTER TERM</strong></td>
<td></td>
</tr>
<tr>
<td><strong>STEP GEN</strong></td>
<td>Applies step generator output to the test fixture emitter terminal and inverts the step generator polarity.</td>
</tr>
<tr>
<td><strong>OPEN (OR EXT)</strong></td>
<td>Disconnects the emitter terminal from the step generator and connects the emitter terminal to the front-panel EXT BASE OR EMIT INPUT terminal.</td>
</tr>
<tr>
<td></td>
<td><em>NOTE: In BASE-GROUNDED mode, the step generator signal at the front-panel STEP GEN OUT is inverted.</em></td>
</tr>
<tr>
<td><strong>EMITTER-BASE BREAKDOWN</strong></td>
<td>Grounds the test fixture base terminal and applies collector sweep voltage (only those supply voltages that are not interlocked) to the emitter terminal. The collector terminal is open in this mode.</td>
</tr>
<tr>
<td><strong>VERTICAL SENSITIVITY</strong></td>
<td>Selects from 26 calibrated vertical deflection factors from 2 nA/DIV to 2A/DIV with mainframe X10 VERT MAG PULL in the &quot;in&quot; position and .2 nA/DIV to 200 mA/DIV with the VERT MAG PULL in the &quot;out&quot; position. All steps follow a 1-2-5 sequence.</td>
</tr>
<tr>
<td><strong>(CURRENT/ DIV)</strong></td>
<td></td>
</tr>
<tr>
<td><strong>LEFT-RIGHT</strong></td>
<td>Three-position toggle switch for applying test signal to either the left or right set of terminal connectors (center position disconnects the terminal connectors). The emitter terminals are connected together and to either ground, step generator, or collector, depending on the position of the Terminal Selector switch.</td>
</tr>
<tr>
<td><strong>Interlock Defeat</strong></td>
<td>In normal operation, collector sweep voltages that are controlled by the interlock are removed from the device under test if the protective cover is open. Pushing the Interlock Defeat button applies sweep voltage with the protective cover open, as long as the button is pressed.</td>
</tr>
<tr>
<td><strong>LOOPING COMPENSATION</strong></td>
<td>Permits compensation of the internal and adapter stray capacitance and for some &quot;device under test&quot; capacitance.</td>
</tr>
</tbody>
</table>
VARIABLE VOLTAGE, VARIABLE OUTPUT
Provides +12, 0-12 continuously variable voltage (referred to ground) to the VARIABLE OUT-PUT connector. Impedance is approximately 10 kohm.

STEP GEN OUTPUT Connector
Provides external access to the step generator output.

EXT BASE OR EMIT INPUT
Provides external access to the base or emitter terminals, depending on the position of the Terminal Selector switch. Also provides a means of connecting an external resistor between the step generator output and base of the device under test.

GROUND
External ground connection.

Table 17: Tektronix Curve Tracer gate Bias Polarity Table

<table>
<thead>
<tr>
<th>Collector Supply Polarity</th>
<th>Step/Offset Polarity button</th>
<th>polarity of gate steps</th>
<th>AID button</th>
<th>Polarity of gate offset initial value</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>in (normal)</td>
<td>+</td>
<td>in (aid)</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>out (oppose)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>out (invert)</td>
<td>-</td>
<td>in (aid)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>out (oppose)</td>
<td>+</td>
</tr>
<tr>
<td>-</td>
<td>in (normal)</td>
<td>-</td>
<td>in (aid)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>out (oppose)</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>out (invert)</td>
<td>+</td>
<td>in (aid)</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>out (oppose)</td>
<td>-</td>
</tr>
</tbody>
</table>

Gate offset initial value is the magnitude of the first voltage applied. The actual applied gate bias is:

\[
V = V_0 + nV_s
\]

where \(V_0\) is the offset voltage, \(n\) is the step (0 to 100), and \(V_s\) is the step size. The signs of these voltages are determined by the table above.