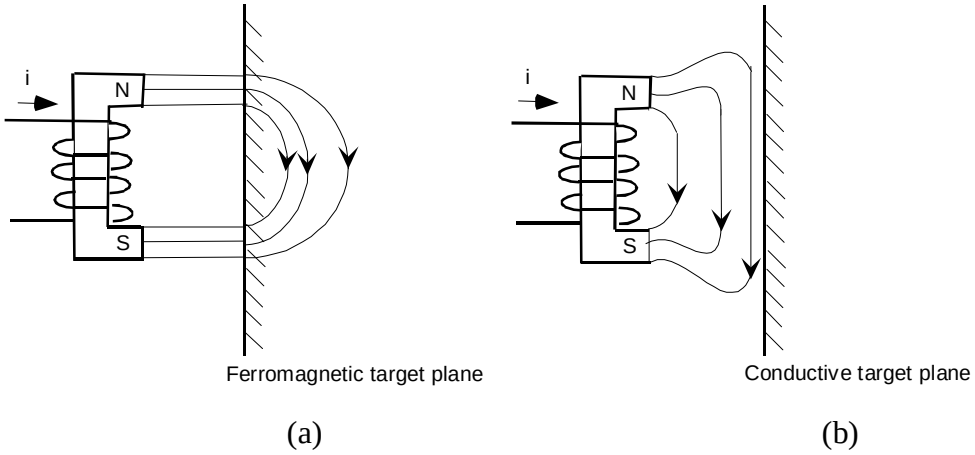
Chapter 1: Introduction

1.1 Inductive Proximity and Distance Sensors

Inductive sensors have been developed commercially as proximity and distance sensors for years. Based on Faraday's law of electromagnetic induction, $V = -N(d\phi/dt)$, these sensors transfer the magnetic information related to the proximity or distance between the sensor and a target to an electrical signal. Faraday's law implies that the varying magnetic flux in a coil with N turns will generate a voltage V at the two ends of the coil. Thus, the basic component of inductive sensors is a coil which generates a magnetic field in front of the sensor and monitors the magnetic field variation when a ferromagnetic or conducting target approaches [1].

For a ferromagnetic target, the reluctance of the magnetic path consisting of the coil and the target decreases and hence the inductance of the coil increases when the distance between the sensor and the target decreases. The magnetic field of a coil sensing a ferromagnetic target is illustrated in Figure 1.1(a). For a conducting target, the magnetic field emerging from the coil induces an eddy current in the approaching target surface. The eddy current creates an opposing magnetic field which is absorbed by the coil according to Ampere's law. Figure 1.1(b) shows the magnetic field of an eddy current sensor. This phenomenon results in a decrease of the inductance of the coil. Therefore, we can measure the inductance of the coil to tell the distance between the coil and the target. The eddy current inductive sensors are more widely applied in industry since the magnetic

field of these sensors penetrates the target only to the level of the orders of skin depth δ, which is approximately equal to $1/\sqrt{pfsm}$, where μ and σ are the permeability and conductivity of the target, respectively, and f is the frequency of the electromagnetic field. As a result, the sensing capability will not be restricted by the thickness of the target if high frequencies are applied.



(a) (b)

Figure 1.1 Magnetic field of a inductive sensor sensing (a) a ferromagnetic and (b) a conductive target.

1.2 INTERFACE CIRCUITRY OF THE INDUCTIVE SENSORS

In addition to the coil components, interface electronic circuits play an important role in extracting the inductance variation with regard to changes in the distance or proximity of the target. The sensitivity of the sensing system can be highly restricted by the interface circuitry. Bridge circuits and oscillators are the two most popular interface circuits for inductive proximity sensors [2].

Wheatstone bridge circuits are used due to their high linearity and temperature compensation. Figure 1.2 is an example of this approach. *Lx* is the

inductance of the sensing coil, and it keeps its balance value of L_1L_2/L_4 to generate a zero output voltage until the presence of a nearby conducting target decreases its inductance to 1-ε. The unbalanced bridge in turn provides an a.c. output voltage the amplitude of which is proportional to the change of the coil inductance ε.

The oscillators are more widely used in industry because of their simplicity [3][4]. A conventional inductive proximity sensor with an oscillator contains three parts: an oscillator circuit, an air-around or ferrite-core inductive coil, and a detector circuit. The oscillator circuit can be either a tuned or relaxation oscillator consisting of a LC tank network in the feedback loop. The inductance and capacitance of the LC circuitry determine the operation frequency of the oscillator. The inductive coil forms the inductance portion of the LC circuit and carries a current, the frequency of which is determined by the oscillator. When an approaching conducting target causes a change in the magnetic field around the sensor, the impedance of the coil is decreased, and therefore either or both the frequency and the amplitude of the oscillator signal change. The change of frequency or amplitude is converted to readable output information through the detector circuit which can be either a Schimitt trigger level detector that generates a digital output and provides target presence/absence information or an analog readout circuit that provides more accurate distance information between the sensor and the metal target. Recently, a differential relaxation oscillator has been proposed [5]. It has the advantages of both the bridge and oscillator circuits and also leads to a high sensitivity.

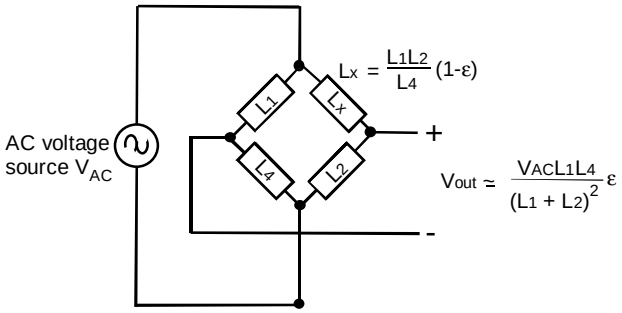


Figure 1.2 A bridge interface circuit with L_x as the inductance of the sensing coil.

1.3 INTEGRATED INDUCTIVE SENSOR SYSTEM

As silicon technologies are developed rapidly nowadays, the compatibility of proximity sensors with microelectronics circuits becomes an important issue. The monolithic integration of the sensing element together with the interface circuit on the same chip is desired to achieve a comparable price/performance ratio with the standard silicon circuits. A miniaturized flat-coil inductor has been proven to be a simple solution in several papers [6][7]. By applying standard process techniques such as CMOS metalization, a coil can be fabricated with integrated interface circuits. When the coil is scaled down, however, the inductance decreases, and as a result, a much higher frequency about $1/m^2$ of the original operation frequency is required to maintain the sensitivity, where m is the scaling factor [8]. Moreover, the downscaling causes a dramatic increase of the serial resistance R_s of the coil due to $R_s = rl/A$, where ρ is the resistivity of the conductor making up the coil, and l and A are respectively the length and cross section of the coil. From the interface circuits' point of view, the serial resistance will behave as a permanent damping element in the LC resonant circuit and

degrade the linearity of the bridge interface circuit because the sensing coil loses its characteristics of a pure inductor with high Q factor.

1.4 TWO-COIL INDUCTIVE PROXIMITY SENSOR DESIGN

A two-coil eddy current proximity sensor has been proposed to avoid the drawbacks of scaling down the sensor system [9]. The two coils build a flat transformer structure in which one coil carries the periodic excitation signals to generate the magnetic field and the other acts as a pick-up coil detecting the magnetic field variation. The separation between the sensor and a metal target is reflected in the phase shift between the electrical signals in the two coils. From the a.c. simulation result of this sensing element model, it is found that the sensitivity of this design is not sensitive to variation in the coils' series resistance. Therefore, the high serial resistance due to scaling down is no longer a concern.

In the conventional proximity sensor system design, there is only one reading, and ideally this reading is a function of only one parameter (distance or proximity). However, in the real world, several components are attributed to the variation of the output reading, and therefore the sensing performance can be degraded dramatically if only one parameter is considered as the variable. To improve the sensitivity of the reading and to get more knowledge of the environment which we want to sense, several studies [1][2] suggest making use of the relationships of the many output variables rather than relying solely on the ideal one-output function of one parameter. In the two-coil sensor design, for a fixed distance between the sensor and a target plate of a certain material, there is an operating frequency at which the sensor achieves its maximum sensitivity to target

proximity. This frequency is found to be related to the conductivity of the target material. Therefore, the conductivity of the target and the frequency for the maximum sensitivity can be regarded as the second input and output of this sensor system, respectively.

The goal of this work is to design an integrated interface circuitry which is capable of meeting the following requirements,

1. extracting both of the two outputs, the operation frequency for the maximum sensitivity f and the phase shift at f with high resolution, in order to get accurate information about both the proximity and the conductivity of the target,
2. keeping the sensor's characteristic independent of the coils' series resistance, and
3. being able to be fabricated monolithically with the two-coil sensor on the same chip by the standard silicon process.

1.5 SUMMARY OF CHAPTERS

Chapter two describes the procedure of drawing the two-coil sensor's SPICE model. The phase response to the frequency of the sensor model as well as the requirement of the input and output stages are also covered.

Chapter three explains how to design the electronic interface circuitry. Two feedback controlling schemes based on a loop consisting of a VCO (voltage controlled oscillator) and a FVC (frequency-to-voltage converter) are elaborated. The performance of each circuit component involved is evaluated by the SPICE simulation.

Chapter four quantifies the characteristics of the sensor and the interface circuitry in terms of sensitivity, resolution and accuracy. The factors causing unsatisfactory results are discussed.

Finally, chapter five summarizes the thesis and addresses additional work to be done in the future.

Chapter 2: Two-Coil Inductive Sensing Element

One-coil inductive sensors have been shown to have serious drawbacks that are caused by the increase in the coil resistance when the coil is scaled down. The two-coil sensor design is a promising alternative.

The basic components of the two-coil inductive proximity sensing system are an exciting coil, a pick-up coil, and a target plate. In this chapter, we will discuss how to build a simple SPICE model out of these three components, and in the following chapters, this model will be used to design and simulate the interface electrical circuit.

2.1 Extraction of the Electric Parameters of a Coil

In this section, only planar rectangular spiral coils are considered. This is because the planar structure can be easily fabricated by the standard CMOS process and because the rectangular spiral coil has been shown to achieve the highest inductance and sensitivity to proximity compared to other geometric coils with the same area [9].

2.1.1 Coil Resistance Calculation

The formula for the resistance of a straight homogeneous material with a resistivity ρ, length l, and uniform cross section A for d.c. current is

$$R = \rho \frac{l}{A}. \tag{2-1}$$

The total coil resistance is calculated by summing the resistance of each segment making up the coil. For a high frequency current, however, Eq. (2-1) will no longer be valid due to the skin depth effect by which the current traveling in the

conductor is confined in a very thin layer, the thickness of which is approximately proportional to the inverse of the square root of the frequency. In this sensor model, the operating frequency range will be shown to be within the range low enough for designers to keep the d.c. formula. Also, the skin depth phenomena has little effect on planar thin-film coils.

2.1.2 Coil Inductance Calculation

The inductance calculation of the rectangular spiral coil is based on Greenhouse's method [10]. The self inductance L_i of a straight conductor segment i with length l_i in microns, thickness t in microns , width w in microns, and relative permeability μ, is

$$L_i = \mathrm{C}\, l_i \left[\ln\left(\frac{2l_i}{GMD}\right) - 1.25 + \frac{AMD}{l_i} + \frac{m}{4}T \right], \tag{2-2}$$

where C is 0.0002 nH μm^{-1} and T is the frequency correction factor (T = 1 for microwave frequencies). GMD and AMD are the geometric mean distance and arithmetic mean distance of segment i, respectively, and they can be found as follows,

$$\ln\left(\frac{GMD}{d}\right) = -\left[\frac{1}{12\left(\frac{d}{w}\right)^2} + \frac{1}{60\left(\frac{d}{w}\right)^4} + \frac{1}{168\left(\frac{d}{w}\right)^6} + \frac{1}{360\left(\frac{d}{w}\right)^8} + \ldots\ldots\ldots \right] \tag{2-3}$$

$$AMD = w + t, \tag{2-4}$$

where d is the distance between conductor filaments of the coil. The mutual inductance between segments i and another segment with the same length a distance d from segment i is

$$M_i = C \bullet l_i \bullet Q_i , \tag{2-5}$$

where Q_i is the mutual-inductance parameter of segment i , obtained from the equation

$$Q_i = \ln\left\{\frac{l_i}{GMD} + \left[1 + \left(\frac{l_i}{GMD}\right)^2\right]^{0.5}\right\} - \left[1 + \left(\frac{GMD}{l_i}\right)^2\right]^{0.5} + \frac{GMD}{l_i} . \tag{2-6}$$

It can be shown that the mutual inductance between two segments is inversely proportional to the distance between them.

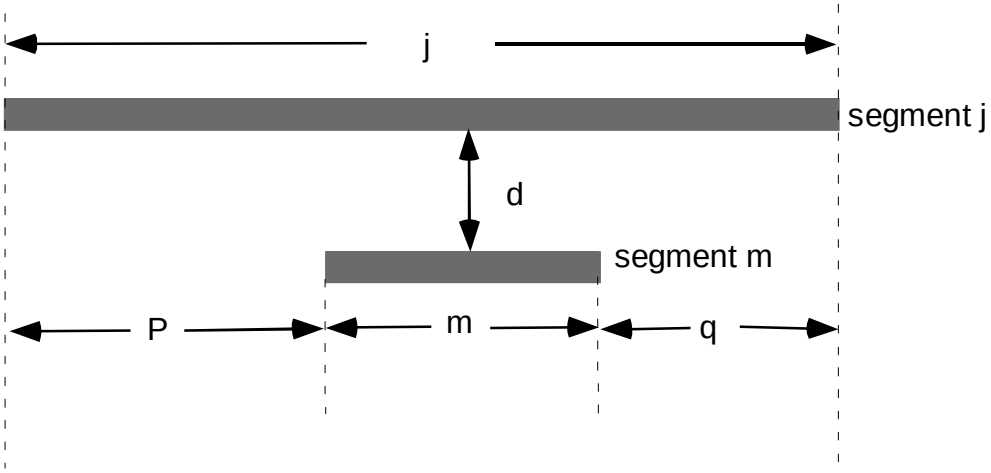


Figure 2.1 Calculation of the mutual inductance between two coil segments with different lengths [10].

So far, it is supposed that each element of the coil has the same length, however, this statement is not valid for most cases. For two segments with different lengths j and m as shown in Figure 2.1, the mutual inductance, $M_{j,m}$, between them is given by the relationship [10]

$$2M_{j,m} = (M_{m+p} + M_{m+q}) - (M_p + M_q), \tag{2-7}$$

where each M term on the right hand side is calculated by Eq.(2-5).

The general expression of the total inductance of a coil is

$$L_{total} = \Sigma L_i + \Sigma M_j - \Sigma M_k \,, \qquad (2\text{-}8)$$

where the first term is the sum of the self inductance of each segment in the coil, and the second and third terms represent the sums of all the positive and negative mutual inductance of each parallel pair of segments, respectively. The mutual inductance is positive when the current flow in two parallel segments is in the same direction or negative when the current flow is in opposite directions. Take a simple rectangular spiral coil shown in Figure 2.2 with a current *I* flowing in the direction of the arrows for example, the total inductance of the coil is

$$L_{total} = L_1 + L_2 + L_3 + L_4 + L_5 - 2\,(M_{1,3} + M_{2,4} + M_{3,5}) + 2M_{1,5} \,, \qquad (2\text{-}9)$$

where each L_i and $M_{i,j}$ are calculated by Eq. (2-2) through Eq. (2-7).

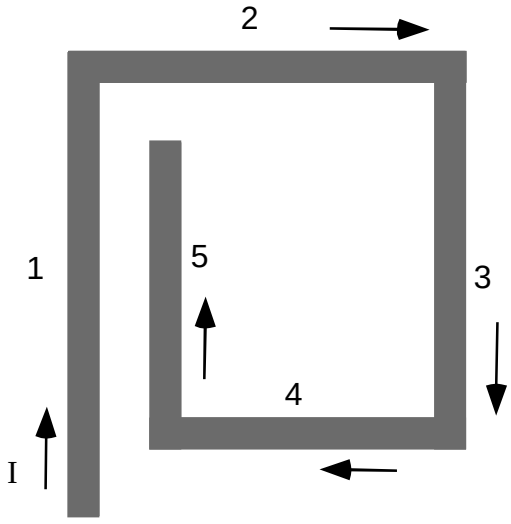
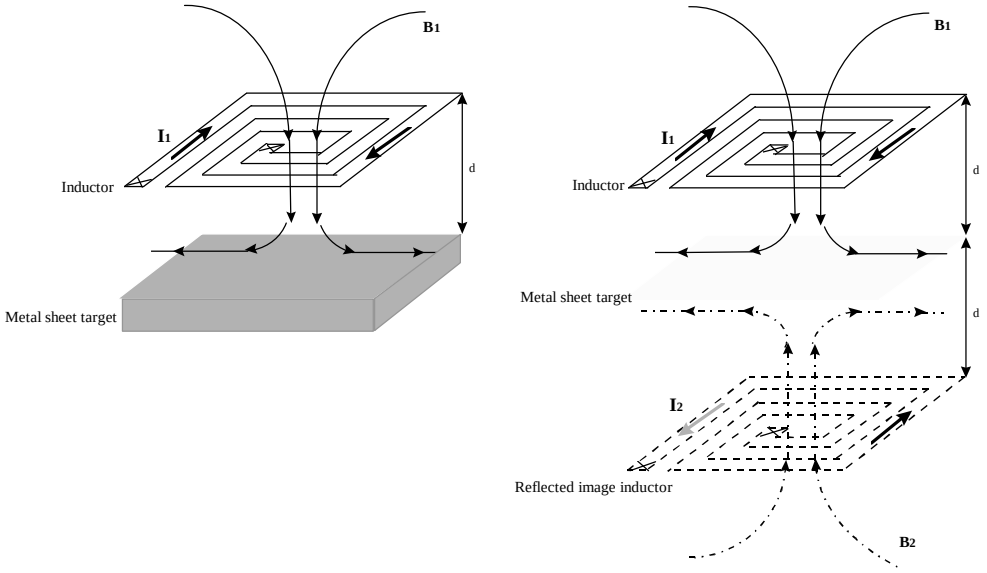


Figure 2.2 An example of a planar rectangular spiral coil .

2.1.3 Calculation of the Mutual Inductance between a Coil and a Conducting Plate

The main function of the inductive proximity sensor is to detect the existence of a conducting plate. The magnetic field generated by the time-varying current flowing in the coil excites the eddy current on the plate. The eddy current then produces a magnetic field normal to the plate, which creates the magnetic flux linkage in the coil. To reduce the complexity of solving the Poisson's equation of this system directly, the method of images is applied instead. By assuming that the plate has zero resistivity and is infinite in extent, the conducting plate can be replaced by the coil's image being placed below the plate surface at a distance equal to the distance between the coil and the plate surface, as drawn in Figure 2.3. The current in the image coil flows in the opposite direction but at the same magnitude as that in the coil. This can be done by imaging the signal source driving the coil to the plate. Therefore, the calculation of the mutual inductance between the coil and the plate placed at a distance d from each other is simplified by the calculation of the mutual inductance between two identical inductors placed $2d$ from each other. This calculation can be evaluated by Eq. (2.3) through Eq. (2.7) if the coil structure is known.



(a) Physical arrangement (b) Application of image theory

Figure 2.3 Illustration of the image theory for a system consisting of a sensing coil and a metal target plate.

2.2 MODELING OF THE TWO-COIL INDUCTIVE SENSOR

The two-coil inductive sensor model is based on the derivation of the one-coil inductive sensor model. So the one-coil modeling algorithm will be discussed at first and then the two-coil model will be drawn out.

2.2.1 One-Coil Inductive Sensor Modeling

According to the method of images, the one-coil sensor with a conducting target plate is present by the transformer circuit model in Figure 2.4. V_i, I_i, R_i, and L_i are the images of V_1, I_1, R_1, and L_1, respectively, so that $V_i = V_1$, $I_i = I_1$, $R_i = R_1$, and $L_i = L_1$. Besides, M_i is the mutual inductance between the coil and its image. The effective inductance of the sensing coil thus is

$L_{eff\_i} = L_1 - M_i.$ (2-10)

The minus sign is a result of the image current traveling in the opposite direction to that of the coil current.

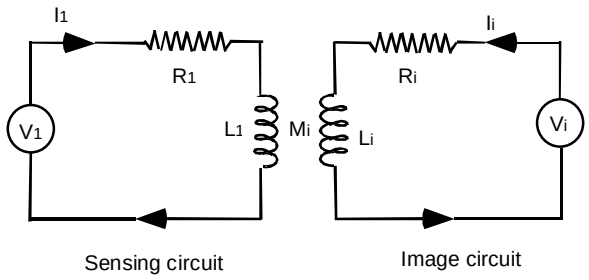


Figure 2.4 One-coil inductive sensor model based on the image theory.

A simplified circuit model [9] is drawn in Figure 2.5. In this case, the image voltage source is removed, and I_s, L_s and R_s are no longer necessarily equal to I_1, L_1 and R_1. The Kirchoff's current loop equations for this circuit are

$I_1 (R_1 + jwL_1) - I_s (jwM_s) = V_1$ (2-11)

$-I_1 (jwM_s) + I_s (R_s + jwL_s) = 0.$ (2-12)

Solving the two equations above, we obtain the effective impedance of the sensing circuit,

$$z_{eff\_s} = \frac{V_1}{I_1} = \left(R_1 + \frac{w^2 M_s^2 R_s}{R_s^2 + w^2 L_s^2} \right) + jw \left(L_1 - \frac{w^2 M_s^2 L_s}{R_s^2 + w^2 L_s^2} \right). \quad (2\text{-}13)$$

The effective impedance can be divided into the imaginary and the real parts as the effective inductance and resistance of the coil, respectively. They are

$$L_{eff\_s} = L_1 - \frac{w^2 M_s^2 L_s}{R_s^2 + w^2 L_s^2} \quad (2\text{-}14)$$

$$R_{eff\_s} = R_1 + \frac{w^2 M_s^2 R_s}{R_s^2 + w^2 L_s^2}. \quad (2\text{-}15)$$

When the frequency ω is much higher than R_s / L_s, the dependence on frequency of R_{eff_s} and L_{eff_s} is eliminated and thus Eq. (2-14) and Eq. (2-15) become

$$L_{eff\_s}' = L_1 - \frac{M_s^2}{L_s} \tag{2-16}$$

$$R_{eff\_s}' = R_1 + \frac{M_s^2 R_s}{L_s^2}. \tag{2-17}$$

In the following sections, it can be verified that ω is almost always much higher than R_s / L_s for the two-coil sensor so that Eq. (2-16) and Eq. (2-17) can always be applied.

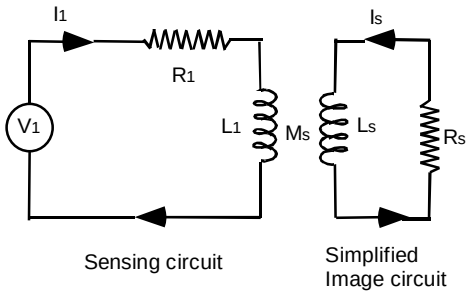


Figure 2.5 Simplified one-coil inductive sensor model.

To force the simplified model in Fig. 2.5 to match the image theory model in Figure 2.4, the effective inductance in two cases must be equal, which implies

$$M_i = \frac{M_s^2}{L_s}. \tag{2-18}$$

This is done by equating Eq. (2-10) and Eq. (2-17).

It is desirable to obtain the values of the parameters M_s, L_s and R_s based on the image theory model the parameters of which are known already. According to Eq. (2-18), it is found that a relation between M_s and L_s is needed to draw these

two parameters from the known M_i. This relation can be acquired as described in the following.

A sensing coil segment with a grounded conducting plane can be connected in two ways as shown in Figure 2.6(a) and (b). Figure 2.6(c) and (d) are the equivalent circuits of the two connection schemes with the method of images applied. The resistance of the coil is neglected to simplify the problem and the image voltage source is removed as the simplified model in Figure 2.5. The effective inductances seen by the voltage source in the two cases are

$$L_{eff\_a} = L_c - \frac{M_g^2}{L_g} \tag{2-19}$$

$$L_{eff\_b} = L_c + L_g - 2M_g, \tag{2-20}$$

respectively, where Eq. (2-19) is derived from Eq. (2-17).

If the grounded plane conductor has infinite conductivity, then the effective inductance seen by the voltage source in the two cases should be the same, which means Eq. (2-19) should be equal to Eq. (2-20). Thus,

$$-\frac{M_g^2}{L_g} = L_g - 2M_g. \tag{2-21}$$

A simple relation between L_g and M_g can be calculated by rearranging Eq. (2-21),

$$L_g = M_g, \tag{2-22}$$

which implies $L_s = M_s$ in the simplified model in Figure (2.5). Moreover, Eq. (2-18) becomes

$$M_i = M_s = L_s. \tag{2-23}$$

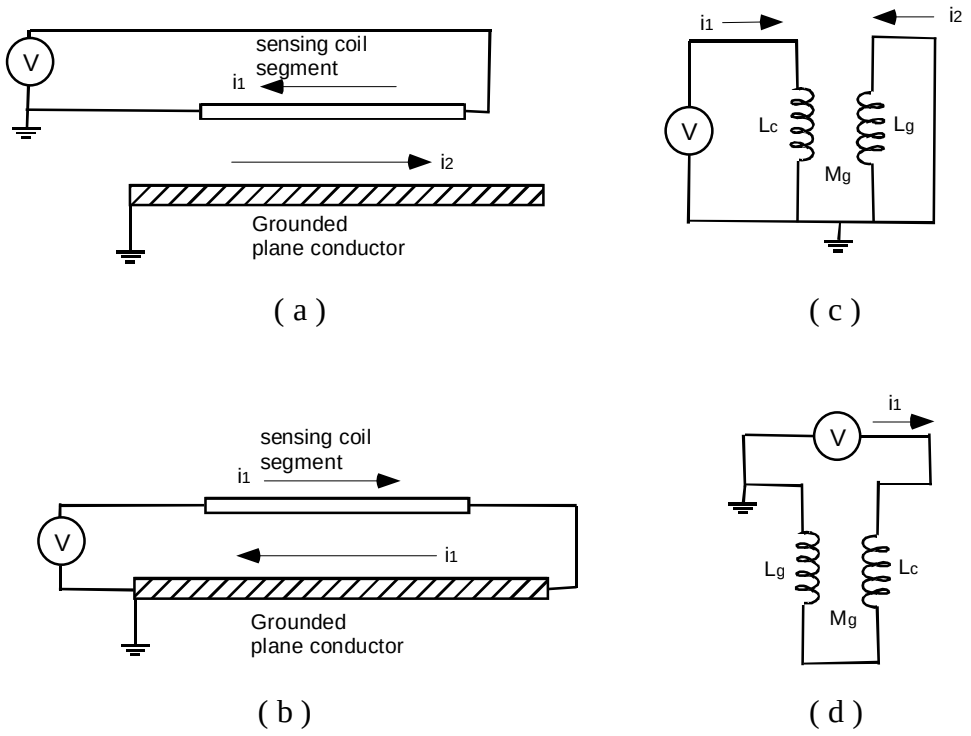


Figure 2.6 Two connection schemes for extracting the sensor model parameters.

For the simplified model in Figure 2.5, R_1 and L_1 can be obtained by the methods indicated in Section 2.1.1 and 2.1.2, and L_s and M_s are equal to M_i which can be calculated by the technique described in Section 2.1.3. The only parameter still unknown is R_s , the resistance of the conducting plate. A quasi-static model for microstrip transmission lines is utilized to calculate R_s. Figure 2.7 shows the structure of this model which consists of a microstrip with a width of *w* over a ground plane at the distance of *h*. The distance *k* is a measure of how long the magnetic fields spread before reaching the ground plane. With $k = 3h + w/2$, the impedance per unit length of the microstrip obtained using this quasi-static model matches that obtained by the full-wave model within 3% [11]. Therefore, a

microstrip over a ground plane can be replaced by a microstrip over a conductor with a width of 6*h* + *w*, and the resistance of the conducting plane below a microstrip is the resistance of a conductor with a width of 6h + w. It should be noted that the plane resistance depends on both the distance between the microstrip and the ground plane and the conductivity of the ground plane.

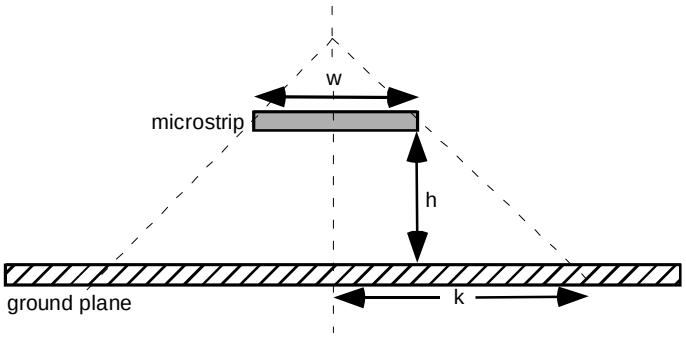


Figure 2.7 Using the model of a microstrip over a ground plane to calculate the resistance of the target plate [11].

2.2.2 Two-Coil Inductive Sensor Modeling

The two-coil inductive proximity sensor has two identical coils, one of which provides the excitation magnetic signals while the other picks up the magnetic signals corresponding to the proximity information of a target plate. Their individual impedance and the mutual inductance between them ($R_{primary}$, $R_{secondary}$, $L_{primary}$, $L_{secondary}$ and M_{12} as shown in Figure 2.8) can be calculated using the method discussed in Section 2.1.1 and 2.1.2. The target plate is modeled based on the simplified one-coil model in Figure 2.5, where L_{plate} is equal to M_{plate} based on Eq. (2.23). The values of M_{plate} and R_{plate} are obtained by the image theory and the quasi-static model mentioned in Section 2.1.3 and 2.2.1, respectively. C_g and

R_g are added as the gap resistor and capacitor between the sensor and the plate because SPICE does not allow the existence of a floating circuit. A very large and a very small value are assigned to R_g and C_g, respectively, in order to eliminate their effects.

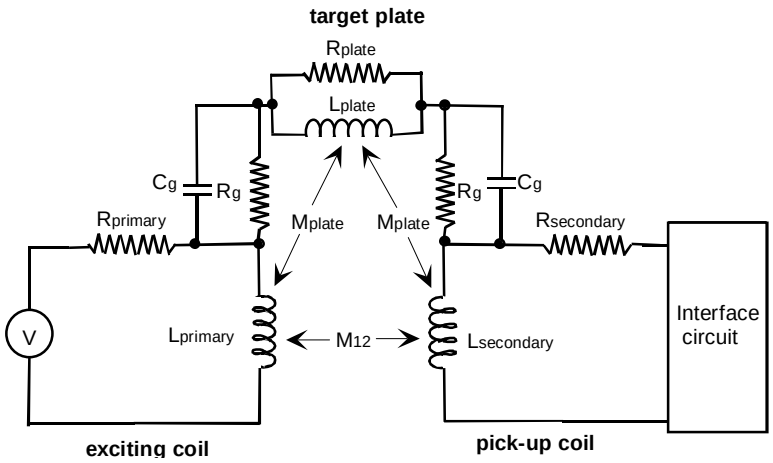


Figure 2.8 The schematic SPICE model of the two-coil sensor with a target plate.

For a certain two-coil sensor design, all the parameters are fixed for any situation except R_{plate} and M_{plate} (also L_{plate}, which has the same value as M_{plate}). M_{plate} relies on the distance between the target plate and the sensor while R_{plate} is related to both the proximity and the conductivity of the target plate. Thus, it can be affirmed that there is a unique solution set of proximity and conductivity of the target for a given set of R_{plate} and M_{plate}. Also, this can explain another reason why the simplified model (Figure 2.5) is preferable to the image model (Figure 2.4). By using the image model, we can only extract the information about the distance of a target, which is ideally a perfect conductor, through the single electronic variable M_i. However, the effects of the nonideal conductivity of the target material are

seen as a reason for the degradation of sensing capability. With the simplified model, the two physical parameters, distance and conductivity of the target, can both be transferred to the magnitudes of the two electronic components, R_{plate} and M_{plate}.

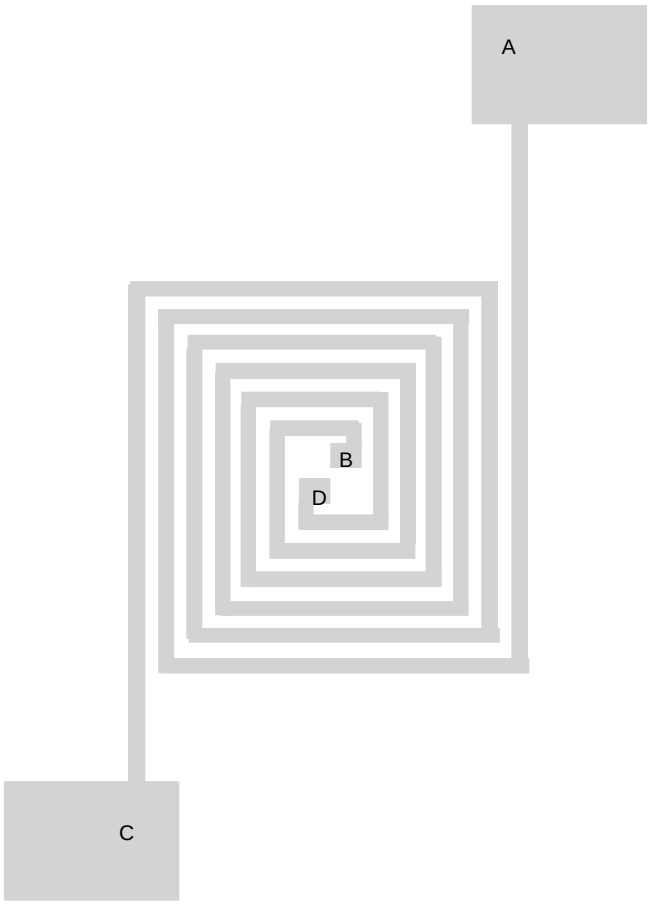


Figure 2.9 The mask design of a planar rectangular spiral two-coil sensor, where A and B are the two terminals of one coil while C and D are the two terminals of the other.

2.3 TWO-COIL INDUCTIVE SENSOR SIMULATION

Ref. [9] has proven that the simulation of the two-coil model is matched quite well to the measurement results of a prototype sensor built on a copper PCB (Figure 2.9). The simulation is done by adding the equivalent circuits of an HP4194A Gain/Phase Analyzer, which is applied to measure the prototype sensor, to the two-coil SPICE model in Figure 2.8. The driving circuit of the HP4194A contains an ideal voltage source and a series resistor, and its detecting circuit is a load resistor. The PSpice® schematic circuit is shown in Figure 2.10. The coupling factor between the two inductors L_1 and L_2 is defined as $M_{12}/\sqrt{L_1 L_2}$, so that the coupling factor between L_{plate} and $L_{primary}$ is

$$k = \frac{M_{plate}}{\sqrt{L_{plate}L_{primary}}} = \frac{L_{plate}}{\sqrt{L_{plate}L_{primary}}} = \sqrt{\frac{L_{plate}}{L_{primary}}} \tag{2-24}$$

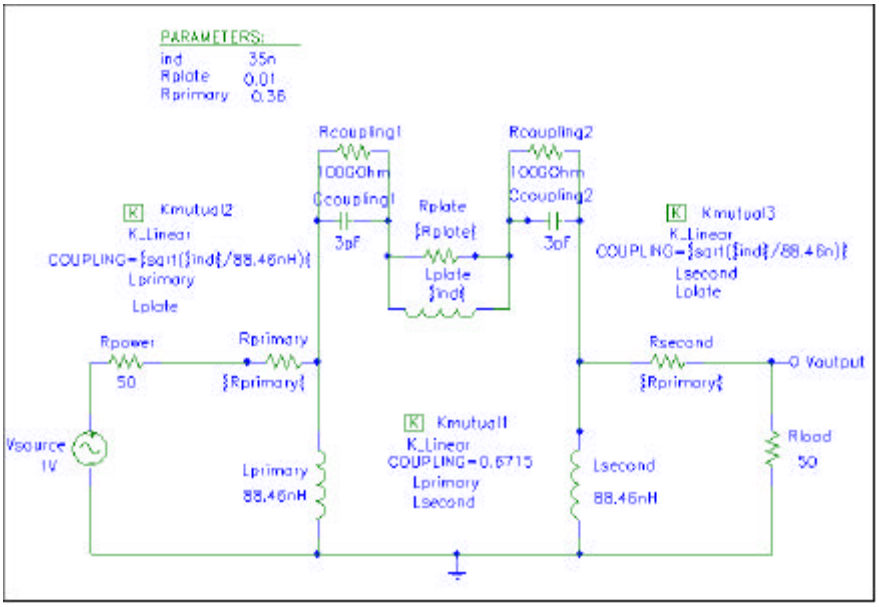


Figure 2.10 The PSpice® schematic circuit of the two-coil sensor together with the equivalent circuit of the HP4194 Gain/Phase Analyzer.

The variation of R_{plate} and L_{plate} is reflected in the phase difference between the electric signals in the pick-up coil and the driving coil. This can be described more precisely as the phase difference between node voltage V_{output} and V_{source} in Figure 2.10. Despite the fact that the gain of V_{output} / V_{source} also depends on R_{plate} and L_{plate}, the gain is generally very low (below -50dB for frequencies lower than 1MHz) and is thus difficult to measure accurately. Figure 2.11(a), (b), and (c) show the influence of the variation of L_{plate}, R_{plate}, and $R_{primary}$ on the phase versus frequency curves, respectively. It is observed that $R_{primary}$ has little effect on the phase shift in the frequency range concerned so that this design is independent of the resistance variation that arises from the process deviation. There exists a minimum phase shift for each concave curve in the frequency range from 10KHz to 1MHz. At the frequency at which the minimum phase shift occurs, the sensitivity of the phase shift to L_{plate} achieves its maximum (Figure 2.11 (a)). The value of the minimum phase shift decreases when L_{plate} increases for a fixed R_{plate}, while the frequency at which the phase shift achieves its minimum increases when R_{plate} increases for a fixed L_{plate} (Figure 2.11(b)). It is desirable to determine the values of L_{plate} and R_{plate} by the minimum phase shift Φ and the frequency f at which the minimum phase shift occurs. However, this can be done only if the system has a unique solution set of L_{plate} and R_{plate} for a measurement result of Φ and f, which will be proved in Chapter 4.

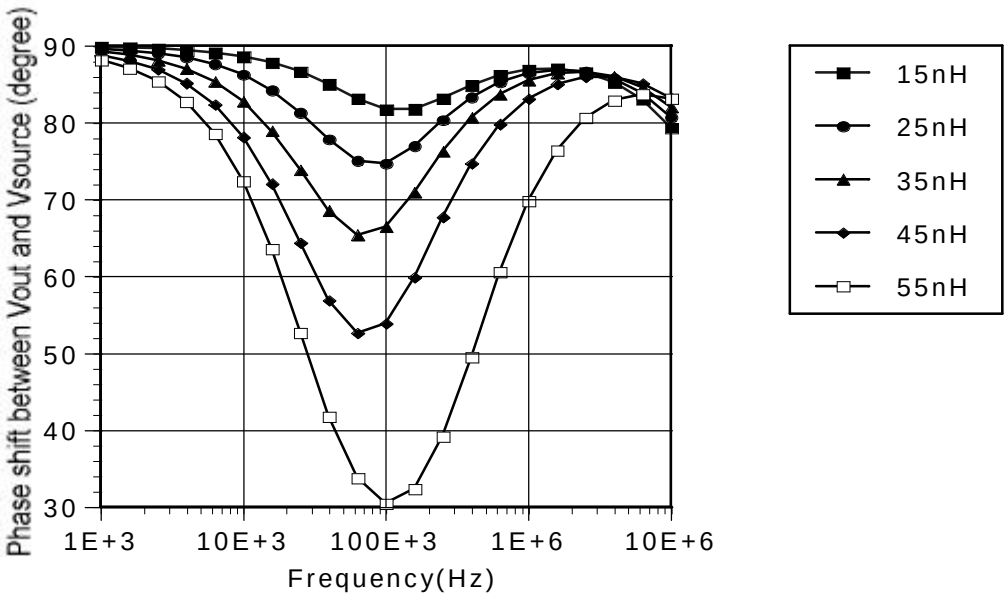


Figure 2.11(a) Simulation of the phase shift between V_{output} and V_{source} with different values of L_{plate}. ($R_{plate} = 0.01\Omega$ and $R_{primary} = 0.36\Omega$)

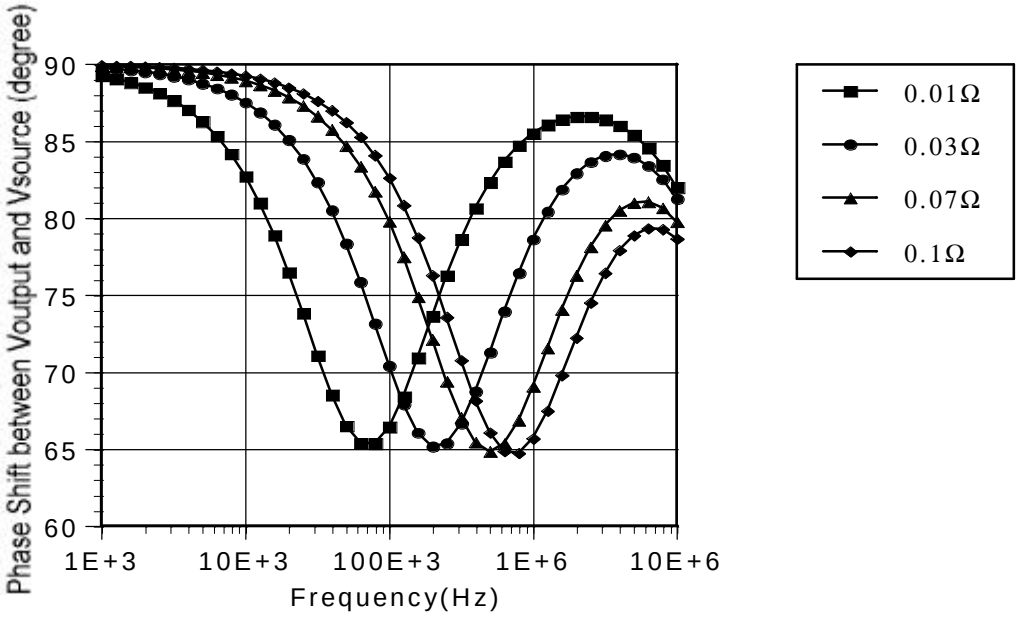


Figure 2.11(b) Simulation of the phase shift between V_{output} and V_{source} with different values of R_{plate}. ($R_{primary} = 0.36\Omega$ and $L_{plate} = 35nH$)

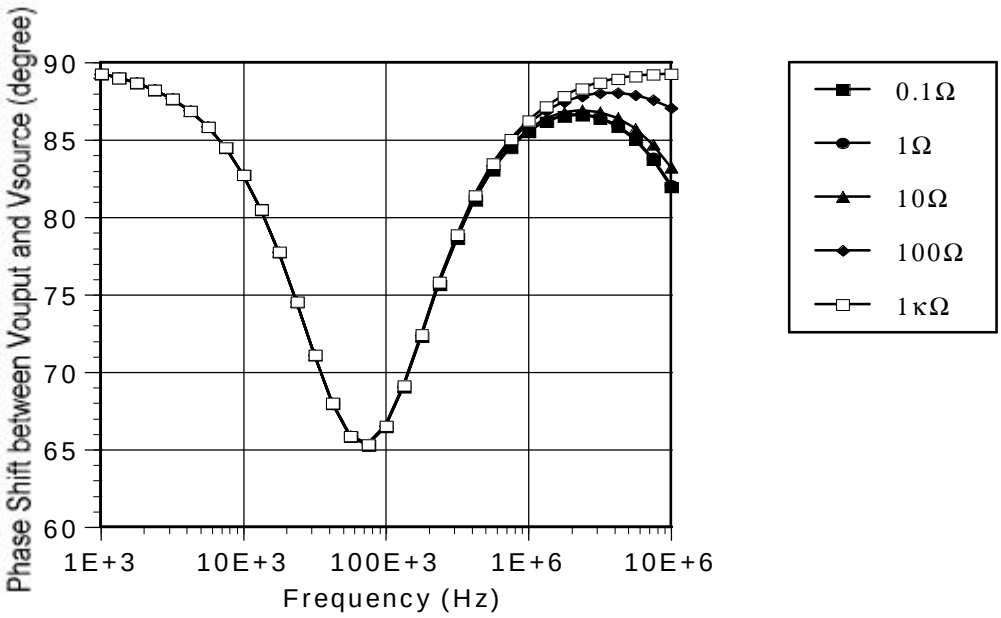


Figure 2.11(c) Simulation of the phase shift between V_{output} and V_{source} with different values of $R_{primary}$. (R_{plate} = 0.01Ω and L_{plate} = 35nH)

2.4 REQUIREMENTS OF THE INPUT AND OUTPUT INTERFACES

In order to design the interface circuit of a two-coil sensor, we need to understand the input and output requirements of the sensing element. For the output requirement, it is obvious that the stage following the sensing element should have a high input impedance to reduce its effect on the sensing performance. For the input circuit, we notice that the driving source of an HP4194A can be replaced by its Norton's equivalent: a current source and a parallel resistance of 50Ω. Since the input impedance of the sensing element is much lower than 50Ω in the relevant frequency range, the parallel resistance of 50Ω can be neglected and therefore the required driving component turns out to be an ideal current source. Moreover, the phase shift between V_{output} and V_{source} in

Figure 2.11 is equivalent to the phase shift between V_{output} and the ideal current source. Since it is impossible to measure the phase of a current directly, a voltage-controlled current source, the current output of which is in phase with the controlling voltage, is more appropriate than a simple current source.

By replacing the driving circuit with an ideal voltage-controlled current source, the simulation results of the phase shift between V_{output} and V_{source} (Figure 2.12) are matched to those in Figure 2.11. The phase shift of $\Phi(V_{output}) - \Phi(V_{source})$ can be divided into two parts,

$$\Phi(V_{output}) - \Phi(V_{source}) = [\ \Phi(V_{output}) - \Phi(V_{in})\ ] + [\ \Phi(V_{in}) - \Phi(V_{source})\ ]. \qquad (2\text{-}25)$$

The first part of Eq.(2-25), which is shown in Figure 2.13(a) and is equivalent to the phase shift between the source and the output voltages if an ideal voltage source is used instead, deviates from the demanded characteristic of a concave-shaped curve and decreases dramatically at higher frequencies. This explains why an ideal voltage source is not desired. The second part of Eq. (2-25), which is equivalent to the phase of the input impedance, increases from zero to 90° as the frequency goes up (Figure 2.13(b)), as a result of that the input impedance of the sensing element is approximately $R_{primary} + j\omega L_{primary}$. The summation of the curves in Figure 2.13(a) and (b) results in the concave-shaped curves as shown in Figure 2.11(a). Besides, both the first and the second parts of Eq. (2-25) vary with $R_{primary}$, but their summation is independent of it.

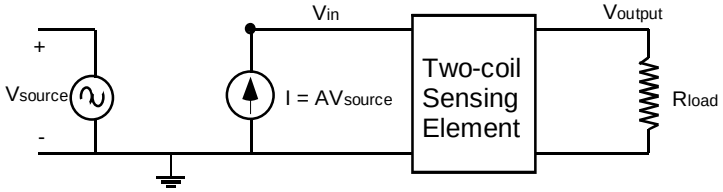


Figure 2.12 Circuit for simulating the sensing element with a ideal voltage-controlled current source as the driving component. (R_{load} = 50Ω)

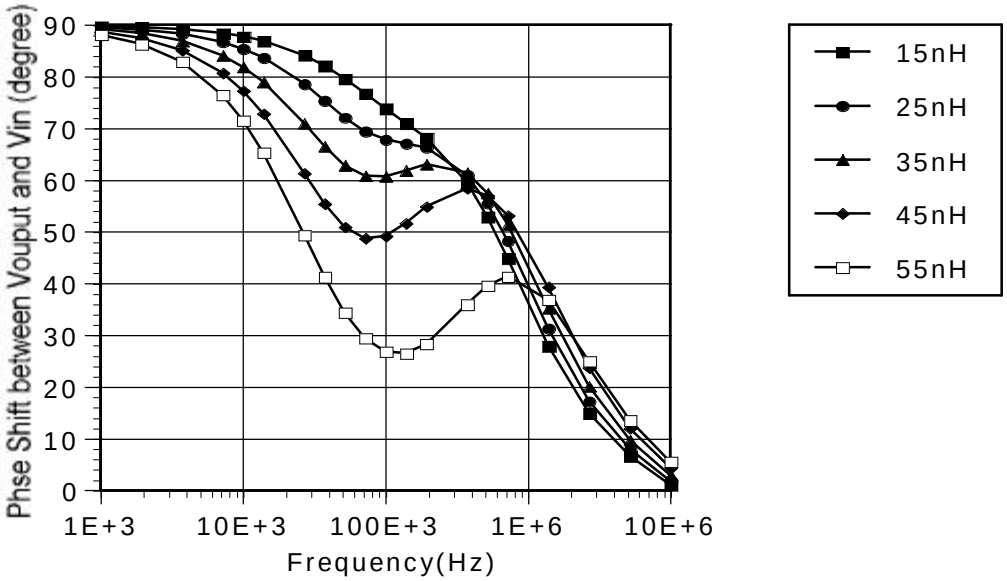


Figure 2.13(a) Simulation of the phase shift between V_{output} and V_{in} in Figure 2.12 with different values of L_{plate} for an ideal voltage controlled current source as the driving circuit. (R_{plate} = 0.01Ω and $R_{primary}$ = 0.36Ω)

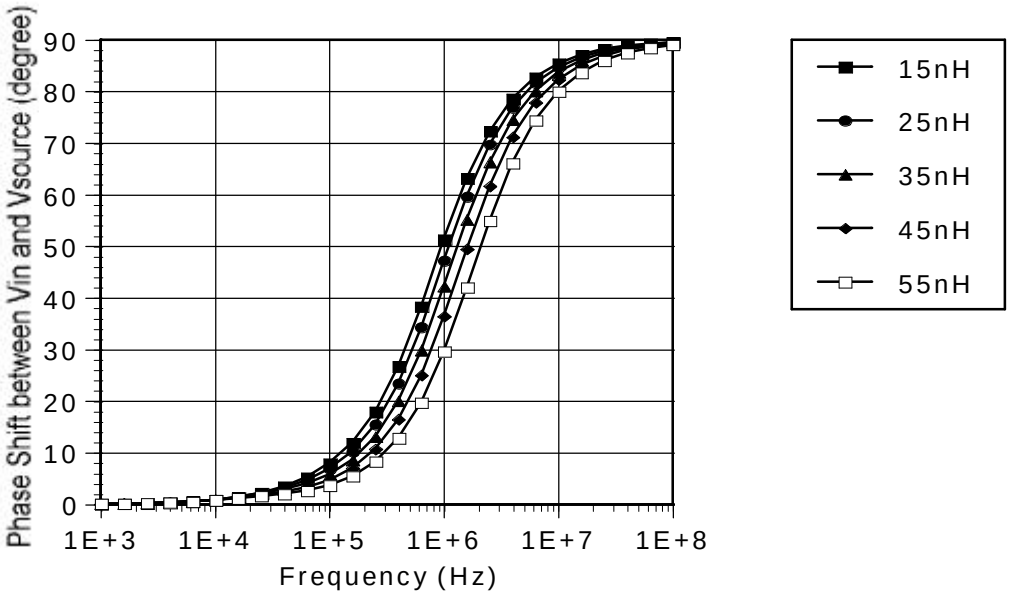


Figure 2.13(b) Simulation of the phase shift between V_{in} and V_{source} in Figure 2.12 with different values of L_{plate} for an ideal voltage controlled current source as the driving circuit. ($R_{plate} = 0.01\Omega$ and $R_{primary} = 0.36\Omega$)

Chapter 3: The Interface Circuit Design

The interface circuit of the two-coil sensor is composed of three parts, a driving circuit, a phase detector, and a feedback loop to adjust the operation frequency to *f*, the frequency at which the minimum phase shift occurs. Two feedback controlling techniques will be discussed in this chapter, and their simulation results will be shown in Chapter 4.

All the circuits mentioned in this chapter are demonstrated by SPICE simulation with the third-level 0.8μm CMOS process models available through the MOSIS services (Table 3.1). The 0.8μm process is chosen because its 5Volt operating voltage is a reasonable magnitude for the analog integrated circuit design compared with 3.3Volt of the 0.35μm process.

MODEL	CMOSN	CMOSP
TYPE	NMOS	PMOS
LEVEL	3	3
VTO	0.663	-1.009
PHI	0.6	0.6
TOX	1.73E-8	1.73E-8
XJ	0.2E-6	0.2E-6
TPG	1	-1
DELTA	9.0290E-1	2.012E+0
LD	7.273E-9	4.546E-9
KP	1.4669E-4	5.6847E-5
UO	734.9	284.8
THETA	4.666E-2	3.303E-1
RSH	2.191E+1	1.817E+1
GAMMA	0.5443	0.4558
NSUB	3.556E+16	2.493E+16
NFS	1.027E+13	1.799E+13
VMAS	1.251E+5	1.444E+5
ETA	8.828E-3	7.081E-2
KAPPA	1.803E-1	2.598E-1
CGDO	2.1776E-11	1.3611E-11
CGSO	2.1776E-11	1.3611E-11
CGBO	4.5116E-10	4.8015E-10
CJ	2.4537E-4	5.5486E-4
MJ	1.0036	0.5099
CJSW	6.8063E-10	1.0633E-10
MJSW	0.332	0.8009
PB	0.8	0.85

Table 3.1 SPICE level 3 parameters of the 0.8 μm CMOS process.

The performance of each circuit component is characterized by its linearity error or accuracy. The linearity error is defined as the maximum deviation of the actual transfer function from the best fitted straight line that describes the output signal, while the accuracy is specified as the ratio of the maximum error of the output signal to the full-scale output signal in a percentage [12].

3.1 INPUT STAGE

As indicated in Chapter 2, the input stage includes a sinusoidal oscillator which provides a frequency ranging from 10KHz to 1MHz and a voltage controlled current source which creates enough power to excite the eddy current in the target plate.

3.1.1 Voltage Controlled Oscillator

Voltage controlled oscillators (VCOs) are widely used for generating untuned operating frequencies. Their outputs are typically square waves and triangle waves, so a sine-shaping circuit is needed to reduce the harmonic contents of the VCO output in this case. Several studies have proposed methods to design a low voltage VCO [13][14][15][16]. According to the consideration of a VCO which can produce a frequency range of two decades (10KHz ~ 1MHz) and can be fabricated by the standard CMOS process, the circuit shown in Figure 3.1 is chosen.

The VCO is based on the operation of the astable multivibrator. M_1, M_2, M_5 and M_6 form a current mirror whose current value corresponds to the input voltage V_{in}. The inverter of M_3 and M_4 is switched by the output of the comparator and sources or sinks current of the magnitude of that in the current

mirror. Due to the basic relationship between the voltage and current on a capacitor for a constant current, I = C ΔV/Δt, the oscillator's frequency can be derived as

$$f = \frac{1}{2\Delta t} = \frac{I_{C1}}{2C_1\Delta V} = \frac{I_{C1}}{2C_1(V_{TRP+} - V_{TRP-})}, \quad (3\text{-}1)$$

where V_{TRP+} and V_{TRP-} are the positive and negative trip points of the comparator with hysteresis, respectively, and the capacitor charging current, I_{C1} is ideally equal to i_1. Because C_1, V_{TRP+} and V_{TRP-} are fixed for a certain design, the oscillating frequency only depends on I_{C1}.

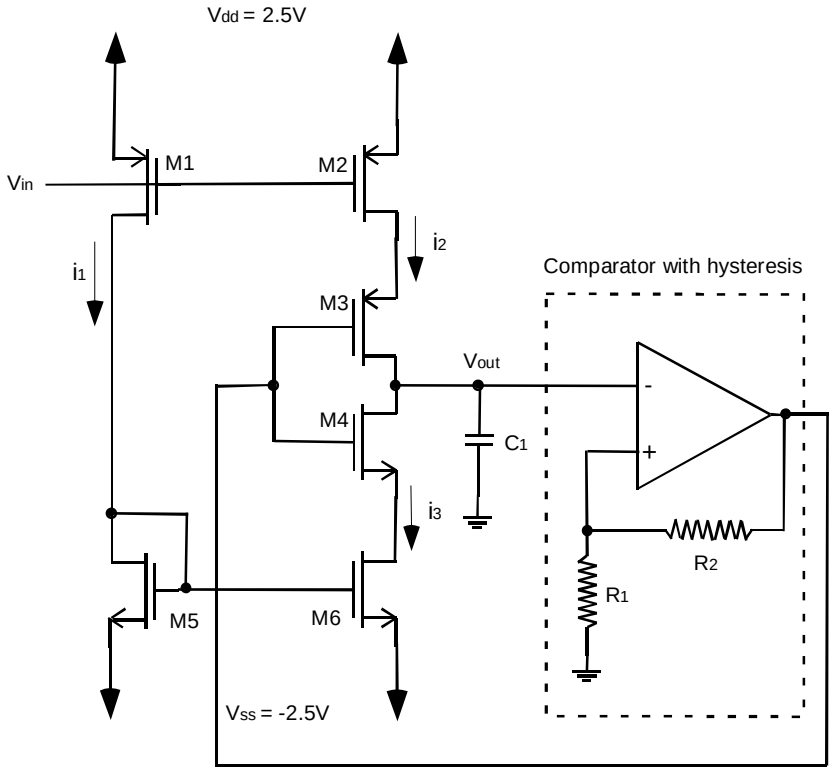


Figure 3.1 Schematic diagram of a VCO compatible with CMOS technology [16].

As the input voltage decreases from Vdd (= 2.5Volt), M_1, M_2, M_5 and M_6 change from the turn-off region to the saturation region and the current in the current mirror increases from zero amperes. This small current guarantees a two decade difference between the minimum current and the maximum current. For the purpose of obtaining a symmetric triangle waveform in the output, the transistors in the current mirror need to be in the saturation region which makes I_1, I_2 and I_3 in Figure 3.1 equivalent to each other via transistor matching. To reduce the magnitudes of V_{GS}, M_3 and M_4 should be assigned higher β, which stands for $\mu_{eff}C_{ox}W/L$, where μ_{eff} is the effective mobility of electrons or holes, C_{ox} is the gate oxide capacitance per area and W/L is the width-to-length ratio of the gate area. Also, the β_3/β_4 ratio must be adjusted to set the trip point of the CMOS inverter at zero volt. When the input voltage continues to decrease, M_1 enters its linear region and the relation between the frequency output and the voltage input is no longer square but linear. Referring to Figure 3.2, the output frequency is roughly a linear function (with linearity error of 18KHz) in the input range from -2.5Volt to 0.6Volt (corresponding to 130KHz to 980MHz in the output frequency) and is proportional to the square of the input voltage for higher input voltage.

For the VCO in Figure 3.1, the gate of either PMOS M_1 or NMOS M_5 can be chosen as the input. Since the active loading MOS (M_5 in our case) of the input stage is always in the saturation region, it should be assigned the kind of MOS which is less susceptible to the channel-length modulation effect. Therefore, the gate of PMOS is chosen to be the input node since the channel-length modulation

parameter of p-channel devices (λ_p) is higher than that of n-channel devices (λ_n) in the model that is applied.

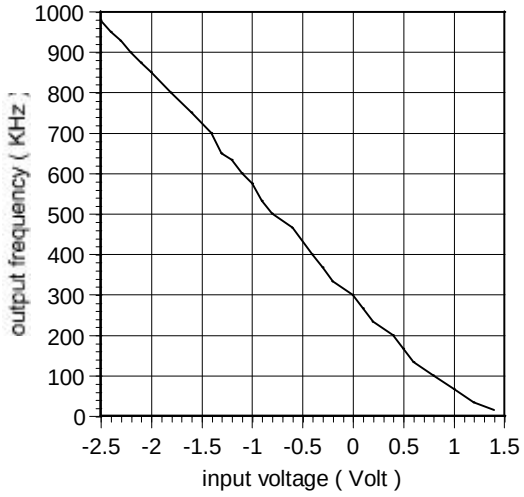


Figure 3.2 Simulation result of the VCO circuit.
(C_1=35pF, $V_{TRP+} = -V_{TRP-}$ = 1.25Volt)

During the SPICE simulation, the VCO output signal may not be a periodic waveform but a d.c. voltage. This problem can be solved by restricting the maximum time step of the transient analysis to a small number via setting the ceiling time step.

3.1.2 Sine-Shaping Circuit

Since the phase shift of the two-coil sensor is very sensitive to the operating frequency, the driving signal needs to have a pure sinusoidal waveform. The triangle waves generated by the VCO have significant odd harmonic contents that are undesirable. It is not practical to apply filters to remove them due to the difficulty of accurately tuning the variable frequencies. Sine-shaping techniques are more commonly used for reducing the harmonic contents of the VCO output.

Instead of diode and bipolar shaping networks which require more sophisticated design and are not appropriate for standard CMOS process, a simple CMOS sine-shaper, shown in Figure 3.3, is used. The square-law differential property of M_3 and M_4 performs the sine-shaping function. The total harmonic distortion (THD), defined as [17]

$$\text{THD} = 100\ \sqrt{\left(D_2^2 + D_3^2 + D_4^2 + ...\right)}\ , \qquad (3\text{-}2)$$

where D_k (k = 2, 3, ..) are the ratios between the amplitude of the kth harmonic and that of the fundamental in the Fourier series representation of the output waveform of the sine-shaping circuit coupled to the VCO mentioned in Section 3.1.1, is plotted as a function of the VCO frequency in Figure 3.4. If a BiCMOS process is available, a refined sine-shaping circuit based on the same differential algorithm but providing a THD under 5% and being independent of the VCO offset voltage, device characteristics and temperature can be built [18]. The transient simulation results of the sinusoidal VCO are plotted in Figure 3.5.

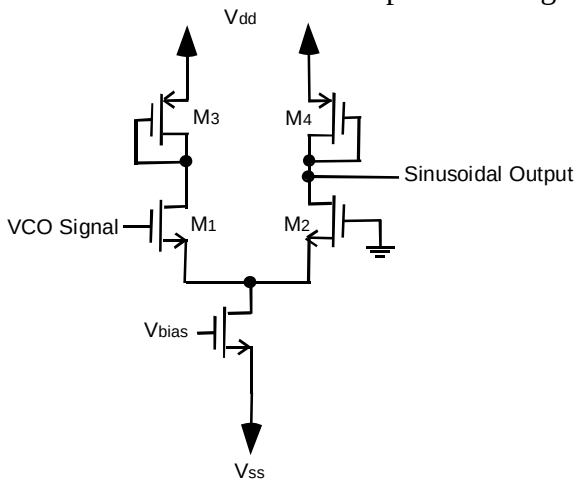


Figure 3.3 Sine-shaping circuit.

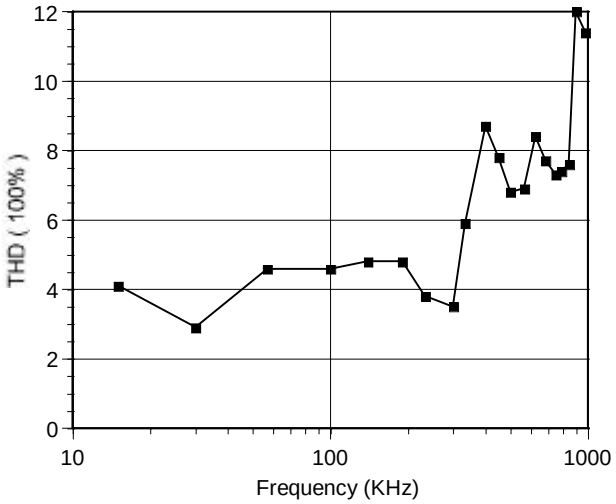


Figure 3.4 THD at the sine-shaper output as a function of VCO frequency.

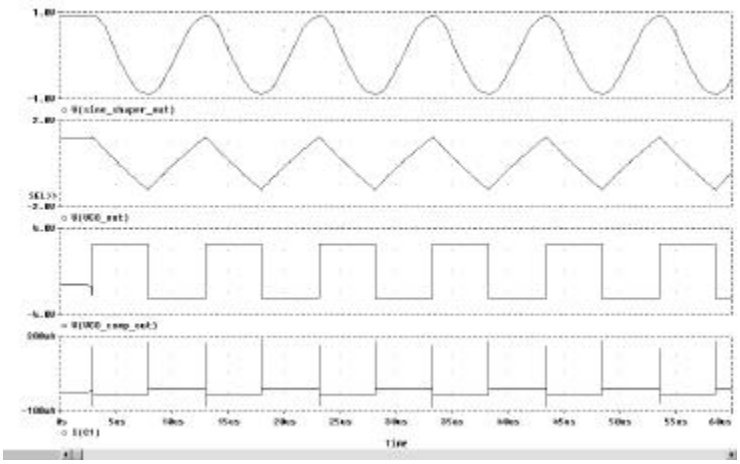
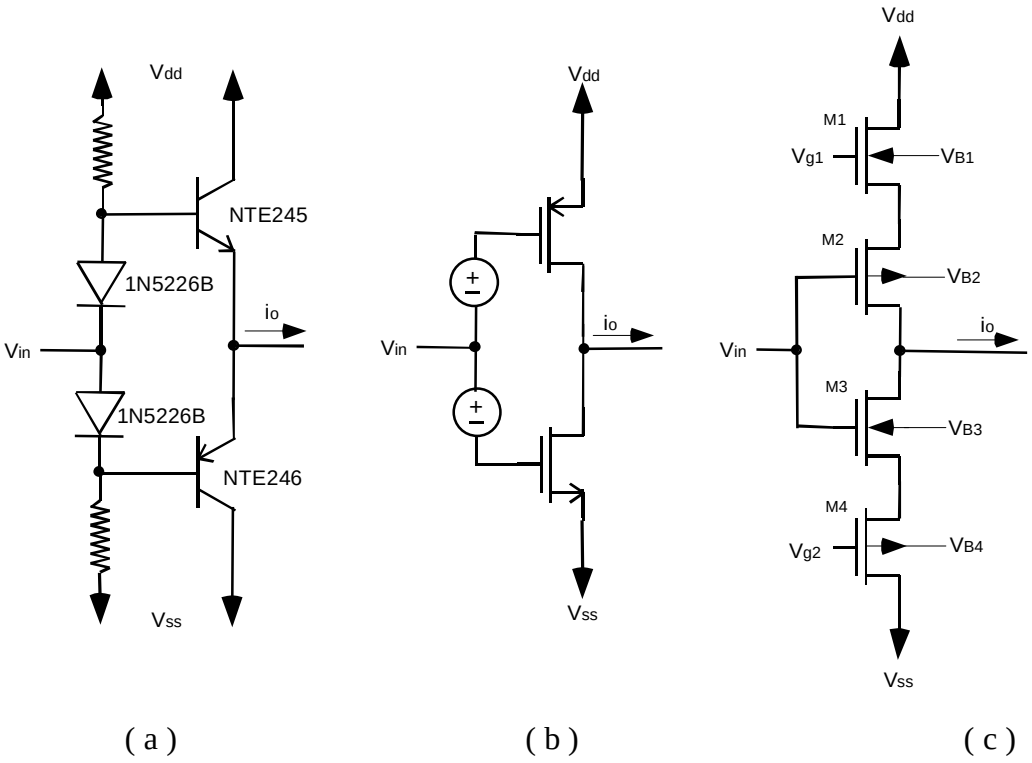


Figure 3.5 The waveform at the sine-shaper output, VCO output, comparator with hysteresis output and the current flowing in the VCO capacitor.

3.1.3 Transconductance Amplifier

The driving circuit for the primary coil requires an ideal voltage-controlled current source which is also called the transconductance amplifier. The class AB output amplifier in Figure 3.6 (a) was formed utilizing discrete components and

was shown to provide enough power to the two-coil sensor by David Lee and David Onsongs [19]. Since the maximum current the two Darlington BJTs (NTE245 and NTE246) can provide is 1 Ampere and the load impedance of the transconductance is below 1Ω, the maximum output swing is ±1Volt – an output swing much lower than the ±15Volt power supply voltages required for the power BJTs to generate 1 Ampere. In this case, the two transistors rather than the primary coil consume most of the power.



(a) (b) (c)

Figure 3.6 Transconductance amplifiers: (a) Class AB BJT output stage (b) Class AB CMOS output stage (c) A linear transconductance element [20].

The two most widely used approaches to designing a transconductance amplifier compatible with CMOS process are a differential stage approach with clever linearizing techniques and a class AB output stage approach illustrated in Figure 3.6 (b). The latter is far simpler than the former; however, its linear performance depends critically on the matching between the NMOS and the PMOS, i.e., $\beta_n = \beta_p$. By replacing each transistor in Figure 3.6 (b) with an NMOS-PMOS pair, as shown in Figure 3.6 (c), the matching between n-channel and p-channel transistors no longer affects the linearity. With identical NMOS devices, M_1 and M_3, and identical PMOS devices, M_2 and M_4, the current flowing through M_2 and M_3 can be derived as [20]

$$I_{M2} = \frac{1}{2}\beta_{eff}\left(V_{g1} - V_{in} - V_{TN1} - |V_{TP2}|\right)^2 \quad (3\text{-}3)$$

$$I_{M3} = \frac{1}{2}\beta_{eff}\left(V_{in} + V_{g2} - V_{TN3} - |V_{TP4}|\right)^2, \quad (3\text{-}4)$$

where

$$\beta_{eff} = b_n b_p / (\sqrt{b_n} + \sqrt{b_p})^2, \quad (3\text{-}5)$$

V_{TN1}, V_{TN3}, V_{TP2}, and V_{TP4} are the threshold voltages of M_1, M_2, M_3 and M_4, respectively. Output current I_o is thus

$$I_o = I_{M2} - I_{M3} = -\beta_{eff}(V_{g1} + V_{g2} - \Sigma V_T)\, V_{in} + \beta_{eff}(V_{g1} + V_{g2} - \Sigma V_T)\, \Delta V_T/2, \quad (3\text{-}6)$$

where

$$\Sigma V_T = V_{TN3} + V_{TN3} + |V_{TP2}| + |V_{TP4}| \quad (3\text{-}7)$$

$$\Delta V_T = (V_{TN3} - V_{TN3}) + (|V_{TP4}| - |V_{TP2}|) + (V_{g1} - V_{g2}). \quad (3\text{-}8)$$

If four wells are used ($V_{BS} = 0$ for each transistor) and $V_{g1} = V_{g2}$, then I_o has an ideal linear relation with V_{in}. However, with a low operation voltage (±2.5Volt), it is difficult to isolate each well from the substrate. So, the two-well structure is

applied here, i.e., $V_{B1} = V_{B3} = V_{ss}$ and $V_{B2} = V_{B4} = V_{dd}$, and thus the body effect causes a nonlinear effect in Eq. (3-6). The d.c. offset and second-order current can be eliminated by appropriately choosing the device dimensions of the n-channel and p-channel devices.

The biasing circuit providing V_{g1} and V_{g2} can be implemented by either a resistive or a MOS voltage divider. If a resistive voltage divider is employed, the resistors of the biasing circuit together with the parasitic capacitors C_{GD} and C_{GS} of the transistors add high order poles and zeros to the phase shift curve in the frequency range discussed in Chapter 2. The additional poles and zeros destroy the concave-shaped curves and are sensitive to the change of the magnitude of the biasing resistors caused by process variation. On the other hand, the equivalent resistance of an MOS voltage divider with the parasitic capacitors of its four transistors can also add a pole, which moves down to the relevant frequency range when the parasitic capacitors increase as a result of the fact that large area MOSFETs are used to provide the 500mA output current. A simple way to avoid adding extra poles or zeros to the phase shift curve is to connect V_{g1} and V_{g2} to V_{dd} and V_{ss}, respectively.

Following the procedure described in [20] to optimize linearity with V_{g1} = 2.5Volt and V_{g2} = -2.5Volt , the relation, $(W/L)_p \cong 5(W/L)_n$, is obtained for the n-channel and p-channel devices in the linear transconductance element. Besides, for the standard CMOS process, the large area transistors can be implemented by connecting several identical small area components in parallel instead of using power devices such as DMOS or VMOS, which require special geometric

configuration or various doping values for different regions [21][22]. This parallel arrangement would result in an output current with the magnitude of the sum of the currents flowing in each channel. The transconductance amplifier consisting of one hundred elements in parallel each with W/L of 1180μm/0.8μm for NMOS and 200μm/0.8μm for PMOS leads to a linearity error of 6.7mA for input voltage within ±0.6Volt and a transconductance of 726mA/Volt. For the a.c. analysis, the phase of the current output is almost equal to that of the voltage input with a maximum error of 0.5 degree.

3.2 OUTPUT STAGE

The output stage is a phase detector which generates a d.c. voltage corresponding to the phase difference between the output signal of the sensing element and the input signal of the transconductance amplifier. A prototype phase detector built in the discrete-component level is analyzed first. Then, a transistor-level phase detector compatible with 0.8μm CMOS process is developed to achieve a monolithic sensor device.

3.2.1 Prototype Design of Discrete Components

The prototype configuration of the output stage, which is shown in Figure 3.7, includes an operational amplifier (LM6265 with a resistive feedback loop), two identical comparators (LM6265), an exclusive-or (XOR) gate (74AC86), a buffer (AD9630), and an integrator (a resistor and a capacitor). LM6265 is chosen to perform the amplification function for the small signal in the pick-up coil because its close-loop frequency response of phase drops only 1° from 0° within

1MHz. This small amount of the phase drop implies that the phase difference between the signal at the pick-up coil and the transconductance input

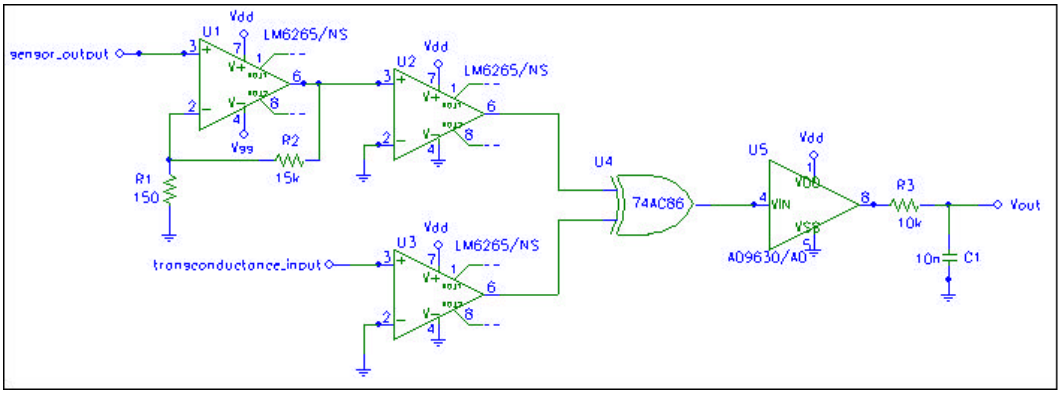


Figure 3.7 Phase detector built by discrete components (V_{dd} = -V_{ss} = 15Volt).

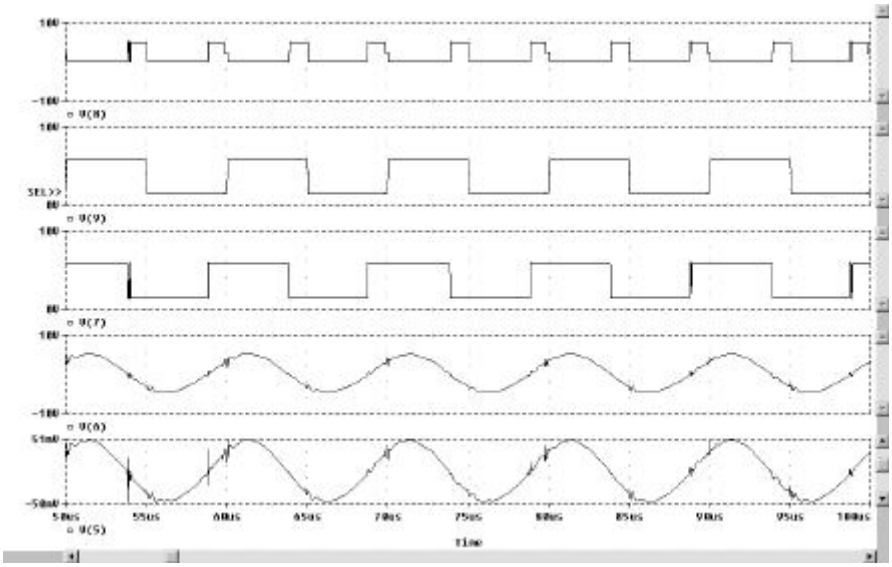


Figure 3.8 Transient simulation results of the prototype phase detector. From bottom to top: waveforms at the pick-up coil, the op-amp output, the first comparator (U2 in Figure 3.7) output, the second comparator out put (U3 in Figure 3.7), and the XOR output.

signal can be taken as the phase difference between the pulses at the outputs of the two comparators with a maximum error of 1°. The XOR gate then produces the absolute difference of the pulses at the two comparator outputs. The ratio of average pulse width over the pulse period of the pulses at the XOR output is proportional to the phase difference between the two comparator output signals. Since the XOR gate is a simple digital component, a buffer is needed to provide enough power to charge the capacitor in the integrator. Finally, the integrator averages the pulse train and generates a d.c. voltage in its settling time. Figure 3.8 explains the operation of the phase detector by showing the waveforms obtained by the circuit simulation with prototype CMOS transconductance element in Figure 3.6 (b) fed by an ideal a.c. voltage signal, R_{plate} = 0.015Ω, L_{plate} = 50nH and $R_{primary}$ = 0.36 Ω.

A good phase detector should perform accurately, linearly and fast. Relating these factors to the prototype circuit described above, it is clear that, ideally, the input offset voltage and the resolution of the comparators and the ripple and the settling time of the integrator should ideally be zero.

3.2.2 Integrated Phase Detector Circuit

The transistor level phase detector structure is generally equivalent to the prototype except that the op-amp of the first stage is taken away because comparators with high gain and accuracy are available.

The open-loop comparator is based on the two-stage structure in Figure 3.9. Three inverter pairs are added to increase the gain and the drive capability, and thus the rise and fall times of the output can be reduced. The first two stages

are connected from -2.5Volt to 2.5Volt because a larger power supply is needed to keep each transistor biased in the saturation region, while the sources of n-channel transistors of the inverter pairs are connected to the ground since the XOR gate requires a non-negative pulse train input. For the XOR gate described in the next paragraph as the load and with one of the inputs connected to the ground, the input offset voltage and resolution of the comparator are 0.55mV and 0.1mV, respectively, and the fall time and rise time are within 10ns in the frequency range of concern. The gain is 25000V/V.

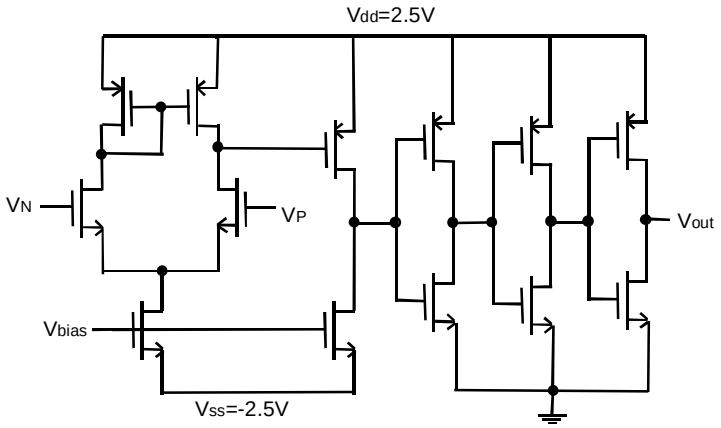
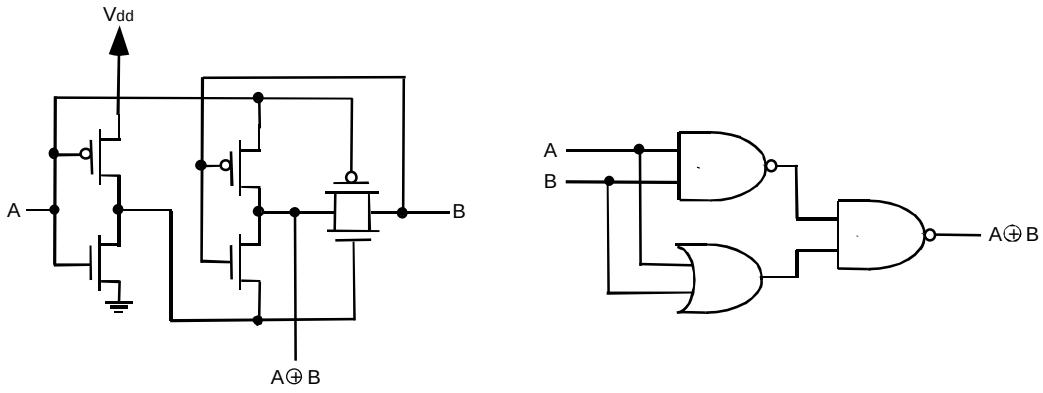


Figure 3.9 Two-stage comparator followed by three inverter pairs.
$V_{out} = A(V_N - V_P)$, where A is the gain of the comparator.

Two schemes to implement XOR gates are examined. The novel one in Figure 3.10 (a) inhabits a much smaller area than that of the conventional XOR gate in Figure 3.10 (b), however, the input impedance of the two input nodes is different so that the phase response of frequency for the two comparators is different. As a result, the phase difference between the two comparator output signals deviates from the phase difference between the transconductance input and

the sensing element output signals. On the other hand, the conventional CMOS XOR gate has approximately the same input impedance for both inputs, and in this case, the two comparator outputs will not interfere with each other during a.c. analysis as they will in the tiny XOR because of the isolation of the high gate impedance at the XOR inputs. The buffer stage following the XOR gate can be easily implemented with several inverter pairs.



(a) (b)

Figure 3.10 Schematics of XOR gate: (a) Transmission gate XOR (tiny XOR) [23] (b) Conventional XOR.

The peak-to-peak ripple voltage and the settling time of the single-pole integrator in the prototype circuit are derived as

$$V_{ripple} \approx T \times I_R / C_1 \quad (3\text{-}9)$$

$$T_{settling} \approx R_3 \times C_1, \quad (3\text{-}10)$$

where T is the period of the operating frequency, C_1 and R_3 are the capacitor and the resistor of the integrator as shown in Figure 3.7, respectively, and I_R is the average current that the buffer provides and is approximately inversely proportional to the integrator resistor R_3. To increase the resolution of the

integrator, low ripples are required; however, decreasing the ripple increases the settling time. This trade-off can be minimized by filtering the single-pole integrator output by a high-order low-pass filter [24]. By this method, the single-pole integrator is designed with high ripples but a fast settling time, and the ripples are then reduced by the high-order low-pass filter. Except for the frequency range below 30KHz, during which the ripples increase dramatically, this approach results in a resolution within 0.004% (with 0.1mVolt of ripple and 2.5Volt full scale output) and a settling time of 2ms, compared with 0.4% (with 60mV of ripple and 15Volt full scale output) and a settling time of 0.5ms for the single-pole design in the prototype circuit. The linearity error is 5mV.

3.3 SUCCESSIVE FEEDBACK LOOP

3.3.1 Theory of Operation

The successive feedback scheme is based on the operation of an HP4194A Gain/Phase Analyzer. The operating frequency scans from an initial value (20KHz, in our case) and increases by a fixed amount in logarithmic scale at each rising edge of the clock pulse until the polarity of the slope of the phase response to the frequency becomes positive. The block diagram and the waveform plotted in Figure 3.11 and Figure 3.12, respectively, illustrate how this feedback loop functions.

The phase detector output is sampled during Clock1 or Clock2 by sample-and-hold circuit 2 or 1, respectively, to store the phase information $V(\phi_{n-1})$ that comes in response to the operating frequency in the previous clock cycle (a clock cycle means half of the period of Clock1 and Clock2). Two control clocks, Clock1

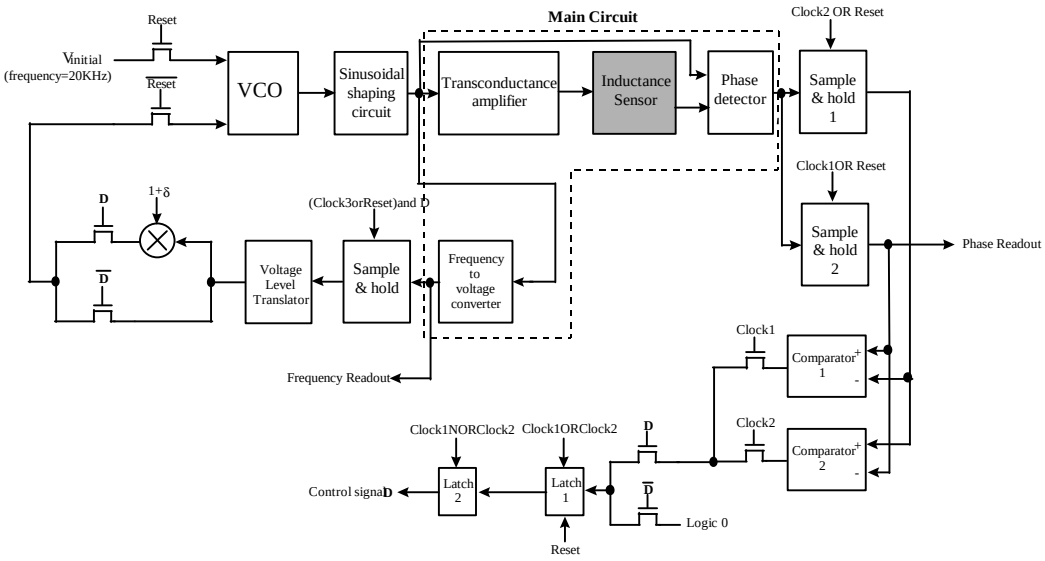


Figure 3.11 Block diagram of the sensor system with successive feedback loop. The dashed line indicates the main circuit which will be discussed in Chapter 4.

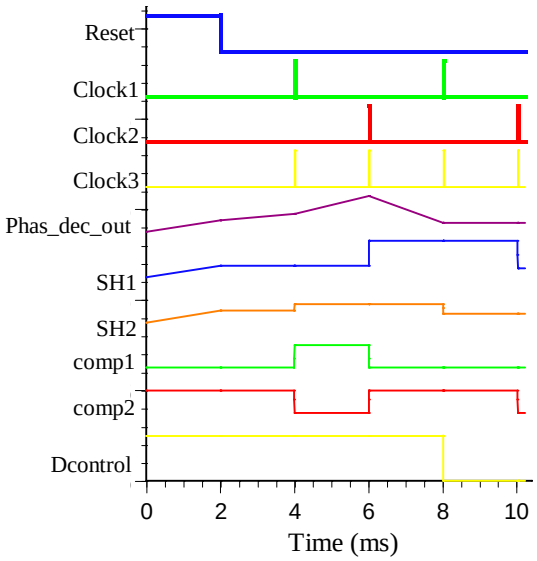


Figure 3.12 Clock and control signal waveforms (From top to bottom: Reset, Clock1, Clock2, Clock3, the outputs of phase detector, sample-and-hold circuit 1, sample-and-hold circuit 2, comparator 1, and comparator 2, and the control signal D as illustrated in Figure 3.11.)

and Clock2, of the same period but with 180° phase difference are needed for sampling the phase detector output because the transit time will result in undesirable charge redistribution in the capacitors of the sample-and-hold circuits and the phase detector if only one clock is used here. The voltage outputs of the two sample-and-hold circuits, $V(\phi_n)$ and $V(\phi_{n-1})$, one of which corresponds to the present operating frequency f_n and the other to the previous one f_{n-1}, are compared by the following comparators. If $V(\phi_n)$ - $V(\phi_{n-1})$ is negative, i.e., the slope of the frequency response of phase shift is negative, the 'D' control signal in Figure 3.11 will be given the value of logic high. On the other hand, if $V(\phi(n))$ - $V(\phi(n-1))$ is positive, i.e., the slope of the frequency response of phase shift becomes positive, the 'D' control signal will change to logic low and keep logic low during all the following clock cycles. The 'D' control signal plays the role of determining whether the operating frequency f_{n+1} of the next cycle should continue to increase in the sub-loop consisting of a VCO and a frequency-to-voltage converter (FVC). During Clock3, which rises right after each pulse of Clock1 and Clock2 with a period determined by the settling time of the phase detector and the FVC, the sample-and-hold circuit in the sub-loop samples the FVC output. Then the sampled voltage increases by timing $1 + \delta$ if the 'D' control signal is logic high or keeps the same value if the 'D' control signal is logic low. A voltage level translator follows to translate the voltage level from the FVC scale (0 to 2.5Volt) to the VCO scale (-2.5Volt to 2.5Volt) and feeds the new voltage value to the VCO, which then converts the voltage to the operating frequency of the next cycle.

Note that the frequency of Clock1 and Clock2 is half of that of Clock3 as a result and the three clocks do not overlap at any time. The pulse width of Clock3 should be short enough to keep the sampled FVC output unchanged with the variation of the VCO input through the feedback loop during the sampling time.

3.3.2 Frequency-to-Voltage Converter

The pulse-integrating FVC is applied here to produce a d.c. voltage linearly proportional to the input frequency. The FVC circuit is based on the configuration of the charge-balancing VFC device, VFC320 of Burr-Brown Corporation [17][24][25], as shown in Figure 3.13. The waveforms are drawn in Figure 3.14. The input comparator (comparator A) converts the sinusoidal waves at the sine-shaping output to square pulses. By suitable biasing, a signal which is insured to cross the zero threshold at each falling edge of the input pulse for any frequency concerned is generated through the coupling capacitor C_1 and triggers the flip-flop built with two NAND gates. The one-shot output of the flip-flop, in turn, closes the switch S_1 and thus pulls a constant current I_{ref} out of the capacitor C_{os} until C_{os} is charged to the reference voltage V_{ref}. The flip-flop then changes its holding value and waits for the next trigger. During this period, C_{os} is discharged to zero through the switch S_2, which is closed by the flip-flop output. The duration T_{os} of the current pulse flowing through C_{os} does not depend on the input frequency but is determined by C_{os}, I_{ref}, and V_{ref},

$$T_{os} = \frac{C_{os} \times |V_{ref}|}{I_{ref}}. \qquad (3\text{-}11)$$

Also, the voltage output V_o is obtained by integrating the one-shot pulse train, which has the duration of T_{os} and the frequency of the sine-shaper output signal.

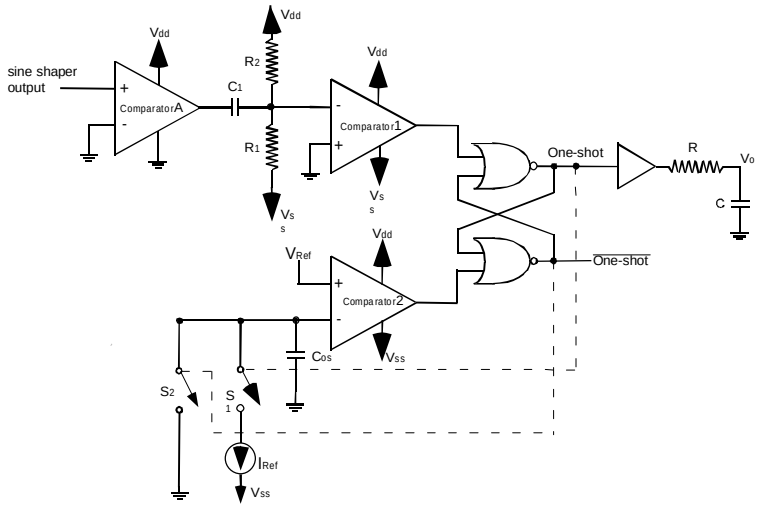


Figure 3.13 Schematic of the FVC.

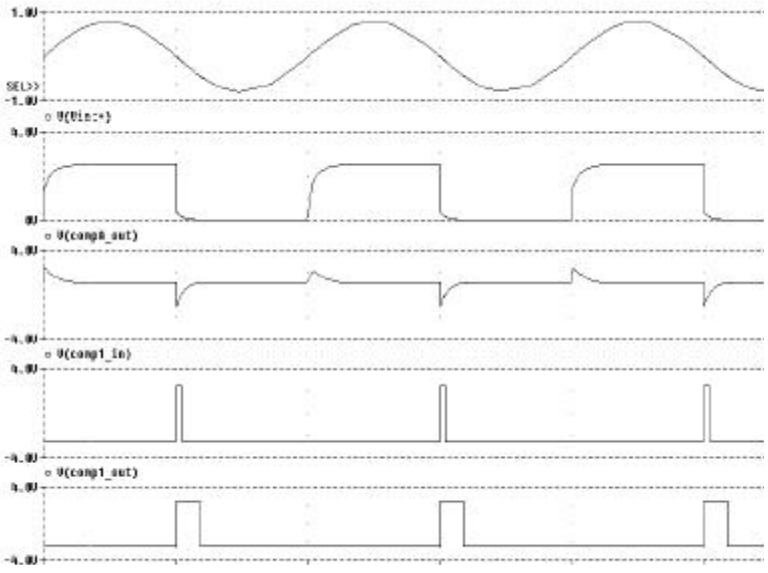


Figure 3.14 Transient simulation results of the FVC. (Form top to bottom: the FVC input, the comparator A output, the comparator 1 input and output, and the one-shot.)

Thus,

$$V_o = V_{dd} \times \frac{T_{os}}{T} = V_{dd} \times T_{os} \times f \ , \qquad (3\text{-}12)$$

where T and f are the period and frequency of the sine-shaper output signal, respectively, and the one-shot signal has the pulse height of V_{dd}, which is 2.5Volt in this case. All the comparators and the integrator are constructed by the same circuit techniques mentioned in Section 3.2.2.

T_{os} has to be no longer than the period of the maximum frequency but long enough to achieve good resolution, i.e., high dV_o/df. By setting C_{os} = 50pF , V_{ref} = -0.5Volt, and I_{ref} = 28μA, T_{os} has the value of 0.886μs and dV_o/df is 2.2mV/KHz. Moreover, the simulation of this FVC results in a linearity error below 2mV.

3.3.3 Sample-and-Hold Circuit

The simple structure of the sample-and-hold circuit applied is shown in Figure 3.15. The capacitor C_H is charged to the input voltage when switch ϕ is closed and holds the voltage when ϕ is open. Since the pulse width of the three clocks controlling the sample-and-hold circuits is 10μs and their periods are 2ms or 4ms, the capacitor C_H has to be small and the switch's driving capability has to be high in order to attain a charging time within 10μs. On the other hand, C_H has to be large enough and the switch's capability of turning-off has to be good enough to hold the charges for a comparably longer time of approximately 2ms or 4ms. Due to this trade-off, the value of the capacitor and the area of the switch should be selected carefully to satisfy both the requirements. Besides, the gate current of the positive input of the op amp should be eliminated to reduce the leakage current during the holding time.

To insure the stability of the feedback loop, the op amp should be compensated properly to attain a phase margin of at least 45°. Moreover, the common mode range (CMR) of the op amp should include the whole possible output range of the phase detector and the FVC. The CMR is defined as the range of common-mode values of the input signals that the op amp continuously senses and amplifies the difference between the two input signals with the same gain [16].

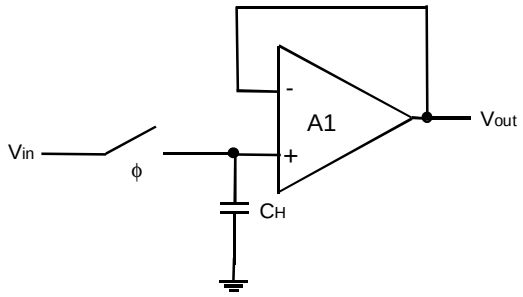


Figure 3.15 Sample-and-hold circuit.

A single NMOS is used as the switch because the sampled voltage is always positive. If a PMOS alone or a CMOS pair is applied instead, the voltage difference between the body, which is connected to the most positive voltage, 2.5Volt, and the drain/source of the PMOS may not be high enough to maintain the inverse-biased p-n junction between them, and thus the undesirable leakage current will become very high. Dummy transistors are used to couple with each single-transistor switch for the purpose of avoiding the clock feedthrough effect. All the switches of sample-and-hold circuits are closed during ‘Reset’ to precharge the capacitors gradually, otherwise the capacitors may not be able to follow the sharp voltage increase during the first clock. For the following clock cycles, the

changes at the outputs of the phase detector and FVC are comparably small due to the small frequency step, so the sample-and-hold circuits can accurately follow the changes.

By carefully designing this system with the 0.8μm process parameters, the sample-and-hold circuit decays by only 1mV during a holding time of 4ms with the accuracy of 1% in the input range from -2.5Volt to 2.3 Volt. Input signals above 2.3Volt exceed the CMR of the op amp, so that the accuracy is degraded to 5%. For the same reason, the voltage level translator has the linearity error of 10mV for the whole input range except for input signals above 2.05Volt for which the linearity error is as high as 0.8Volt.

3.4 ITERATIVE FEEDBACK LOOP

Instead of the fixed frequency steps in logarithmic scale for the successive feedback scheme, the iterative feedback loop generates frequency steps that are determined by the outputs of the phase detector and FVC during the last two clock cycles. Besides, the frequency step can be either positive or negative as opposed to the unidirectional characteristic of the successive feedback loop.

3.4.1 Theory of Operation

The block diagram of this design is drawn in Figure 3.16. Both the phase detector and FVC have two sample-and-hold circuits that sample their output voltages in turn by applying the same clock signals, Clock1 and Clock2, as those used to control the switches in the successive feedback loop. Thus the phase information Φ_{n-1} and Φ_{n-2} and the frequencies f_{n-1} and f_{n-2} for the last two clock cycles can be stored in the form of voltage. An analog computer takes the outputs

of the four sample-and-hold circuits as its input signals and Clock1 and Clock2 as its control signals and calculates the frequency step $D f_n$ for the next clock cycle. At the end of Clock1 or Clock2, the summation of $D f_n$ and the last frequency f_{n-1} is saved as a voltage value in the sample-and-hold circuit 6. During Clock3, which is the same as Clock3 in the successive feedback design, the sample-and-hold circuit 5 samples the voltage containing the frequency information for the next clock cycle and feeds it into the VCO.

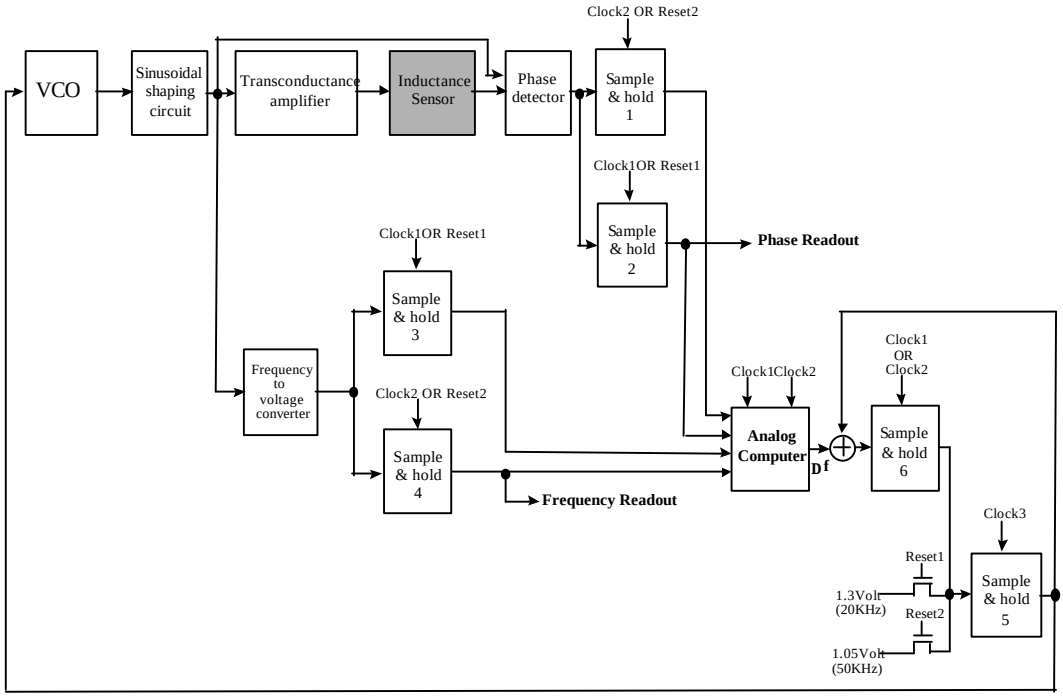


Figure 3.16 Block diagram of the sensor system with iterative feedback loop.

It is obvious that the magnitude of the frequency step $D f_n$ should be proportional to the last frequency f_{n-1} and increases when the difference between Φ_{n-1} and Φ_{n-2} increases according to the Newton-Raphson iteration. $D f_n$ also increases

with the last phase shift Φ_{n-1}. This will be explained in Chapter 4. Thus, the transfer function of the analog computer has the form of

$$\left|\Delta f_n\right| = C \times (f_{n-1} + A) \times (\left|\Phi_{n-2} - \Phi_{n-1}\right| + B)^k \times (\Phi_{n-1} + D)^l, \quad (3\text{-}13)$$

where A, B,... and l are unknown coefficients and constants. The polarity of $D\ f_n$ is determined by that of $\Phi_{n-2} - \Phi_{n-1}$ and that of $f_{n-1} - f_{n-2}$. And for the same Φ_{n-1}, Φ_{n-2}, f_{n-1} and f_{n-2}, the magnitude of positive $D\ f_n$ should be larger than that for negative $D\ f_n$ because the approximately symmetric concave curve of the phase shift is drawn in a logarithmic scale of the frequency. Besides, we should prevent the operating frequency from sticking to the maximum frequency (1MHz).

The coefficients and constants of the transfer function are obtained by trial-and-error on the spreadsheet until the lowest number of the average clock cycles required for $|D\ f_n|$ to converge and for the frequency variation to be below the variation tolerance is achieved. The output $D\ f_n$ is thus

$$\Delta f_n = \Delta f_{no} \times IF(\Delta f_{no} > 0,\ 1\ ,\ 1/2.45) \times IF\ (\ f_{n-1} = 1\text{MHz}\ \textit{and}\ D\ f_{no} > 0\ ,\ -1/2.45\ ,\ 1\ ), \quad (3\text{-}14)$$

where

$$\Delta f_{no} = 0.0028 \times (f_{n-1} + 10) \times \sqrt{\left|\Phi_{n-2} - \Phi_{n-1}\right|} \times (\Phi_{n-1} + 35)$$
$$\times IF(\Phi_{n-2} - \Phi_{n-1} > 0,\ 1\ ,\ -1)$$
$$\times IF(\ f_{n-1} - f_{n-2} > 0,\ 1\ ,\ -1\ ), \quad (3\text{-}15)$$

and *IF(A, x, y)* is *x* if *A* is true and *y* otherwise. The circuit implementation of this analog computer is shown in Figure 3.17. $\Phi_{n-1} - \Phi_{n-2}$ is calculated by the difference amplifier shown in Figure 3.18. This instrumentation amplifier configuration ensures that the input impedance seen by each input is ideally infinite, and its

accuracy is 0.1% in the phase shift range concerned (25° to 85°). The square root and multiplication computation are performed by the multifunction converters, which will be described in the next section. Note that all the frequency and phase terms in Eq. (3-14) and Eq. (3-15) have to be converted to voltages through the transfer functions of the FVC and the phase detector to propagate in the voltage-based analog computer. And the output $D\,f$ in Figure 3.18 is an analog voltage signal corresponding to the frequency step through the VCO transfer function. As a result, the linearity of the transfer function of the FVC, VCO and phase detector will have a serious influence on the accuracy of the analog computer.

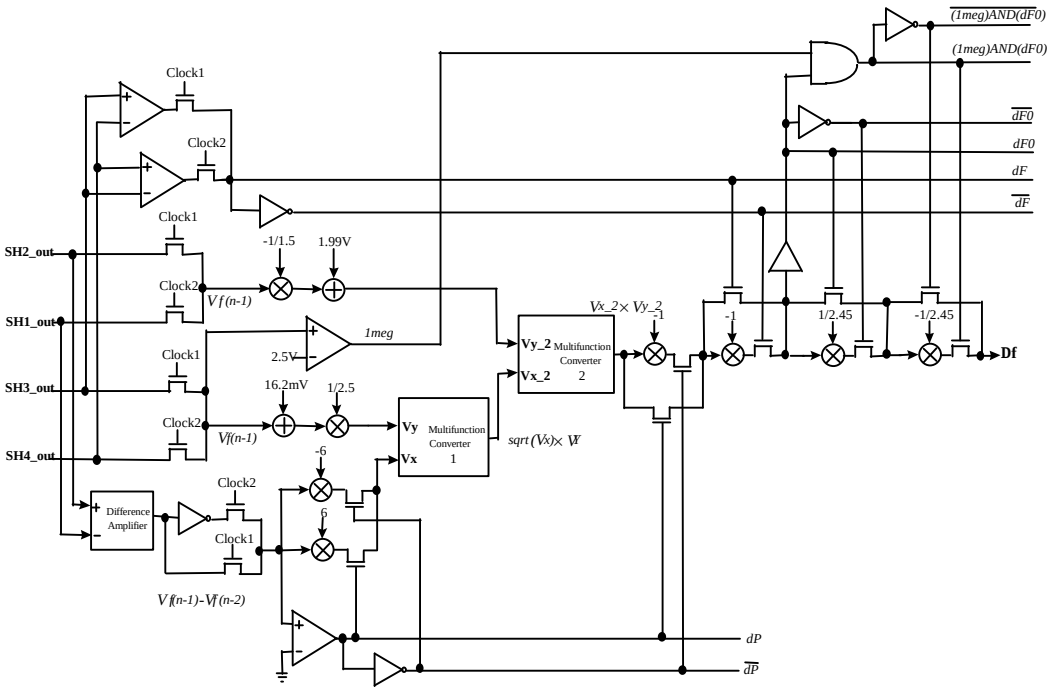


Figure 3.17 Schematic of the analog computer.

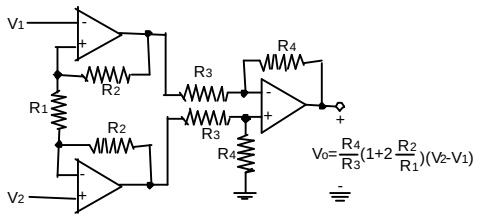


Figure 3.18 Schematic of the difference amplifier.

3.4.2 Multifunction Converter

The multifunction converter is based on the fundamental architecture of two devices, LH0094 of National Semiconductor and 4302 of Burr-Brown Corporation [17][26], as shown in Figure 3.19 (a). Four external discrete bipolar transistors (MM5262) with very low threshold voltage to satisfy the low power supply requirement are added to the integrated circuit simulated. Knowing that the negative input node of each op amp can be taken as virtual ground, we get

$$I_x = \frac{V_x}{R_x}\ , \quad I_y = \frac{V_y}{R_y}\ , \quad I_x = \frac{V_x}{R_x}\ , \quad I_o = \frac{V_o}{R_o}. \tag{3-16}$$

By setting all the resistors of the same magnitude (10KΩ), the ratio between any two currents is equal to the one that exists between their corresponding voltages. The exponential I-V characteristic of the bipolar transistors gives the following relations,

$$I_o = I_s \exp\left(\frac{V_1 - V_{A_y\_out}}{V_T}\right) \tag{3-17}$$

$$I_y = I_s \exp\left(\frac{-V_{A_y\_out}}{V_T}\right). \tag{3-18}$$

Dividing Eq. (3-17) by Eq. (3-18) and rearranging the terms, we obtain

$$V_1 = V_T \ln\left(\frac{I_o}{I_y}\right). \tag{3-19}$$

By the same method, V3 can be written as

$$V_3 = V_T \ln\left(\frac{I_z}{I_x}\right). \tag{3-20}$$

With $R_1 = R_2 = 50\Omega$ in Figure 3.19 (b), $V_3 = 0.5\ V_1$, so that Eq. (3-19) and Eq. (3-20) together yields $(I_o / I_y) = (I_z / I_x)^{1/2}$, which implies

$$V_o = V_y\left(\frac{Vz}{Vx}\right)^{\frac{1}{2}}. \tag{3-21}$$

The square root of V_z can therefore be computed by setting V_z and V_x equal to 1Volt. For the multiplication computation, letting $V_3 = V_1$ as shown in Figure 3.19 (c) and thus equalizing Eq. (3-19) and Eq. (3-20), we obtain

$$V_o = V_y\left(\frac{Vz}{Vx}\right). \tag{3-22}$$

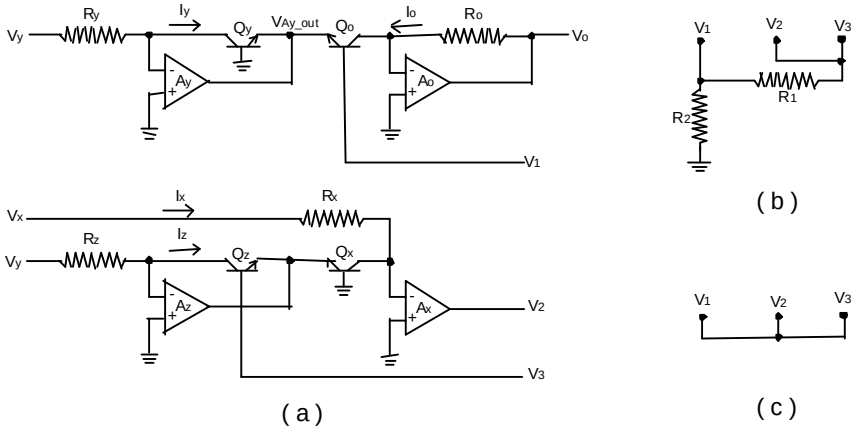


Figure 3.19 (a)General schematic of the multifunction converter and node arrangements for (b) square root extractor and (c) multiplier.

Figure 3.20 and 3.21 show the accuracy of the circuit in computing the square root and in the multiplication modes, respectively. The accuracy can be better than 1%

if the input signals are converted to 1Volt full scale before being fed to the multifunction converter.

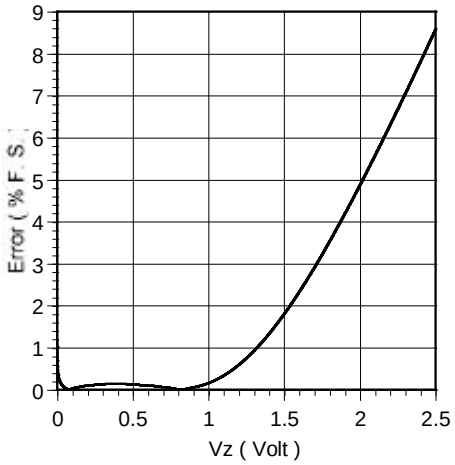


Figure 3.20 Performance of the multifunction converter in square root computing mode.

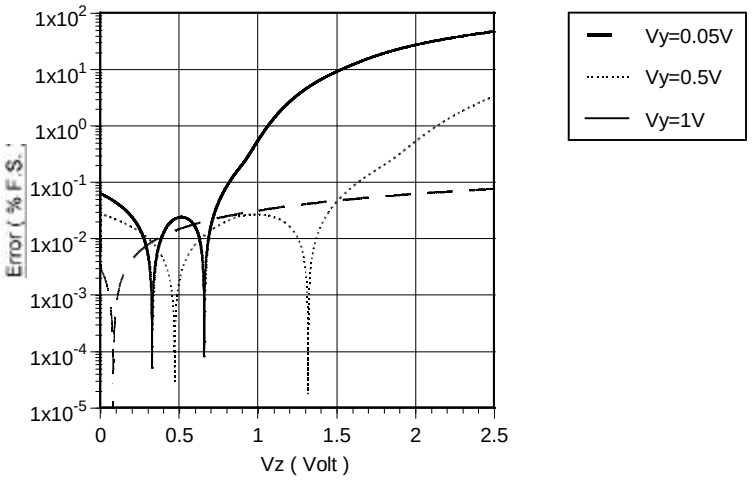


Figure 3.21 Performance of the multifunction converter in multiply mode.

During the SPICE simulation, stability problems can occur in the iterative feedback circuit even though each op amp employed is compensated properly. The use of large bypass capacitors with one end connected to the negative inputs of the op amps A_z and A_y in Figure 3.19 (a) and the other connected to ground can enhance the stability.

Chapter 4: Characteristics of the Sensor and the Interface Circuits

In this chapter, we will describe the performance of the sensor and the interface circuits by referring to the SPICE simulation results. The sensitivity of the sensing element with an ideal voltage-controlled current source as the input will be quantified at first, and then the resolution of the main circuit in Figure 3.11 with an input of an ideal voltage source will be determined. Finally, the successive and iterative feedback schemes will be examined by the transient analysis.

4.1 Sensitivity of the Sensor with an Ideal Input Stage

The definition of sensitivity is the ratio of the change of the electronic output signal to the change of the physical measurand [12]. Generally, it is desirable that the change of an output signal is caused by only one measurand so that the output readout can be converted to a physical quantity easily and accurately. The two-coil sensor system that we are interested in has two output signals, the minimum phase shift and the frequency at which the minimum phase shift occurs, and two measurands, resistance and inductance (R_{plate} and L_{plate}) of the target plate, as indicated in Chapter 2. The a.c. analysis is applied to the circuit configuration illustrated in Figure 2.11 in order to understand how these output parameters relate to the measurands. The simulation results are given in Figure 4.1 and Figure 4.2. It is observed that the minimum phase shift is independent of the resistance of the target plate. This means that if a pair of electrical output signals is measured, a unique pair of R_{plate} and L_{plate} measurands can be determined. The average sensitivity of the minimum phase shift to the target plate inductance is 1.14 degree/nH with a linearity of 8 degrees. The linearity is not so ideal, but in this

case, this phenomenon will not have any significant effect on the sensing performance nor does it degrade the functioning of the interface circuit.

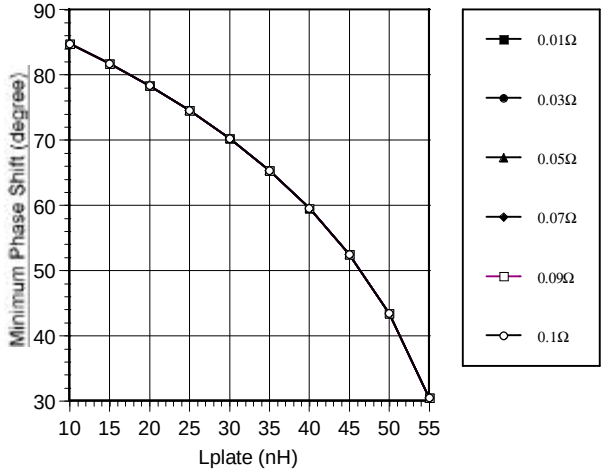


Figure 4.1 The minimum phase shift vs. the target plate inductance for diverse fixed values of the target plate resistance. The input stage is an ideal voltage-controlled current source.

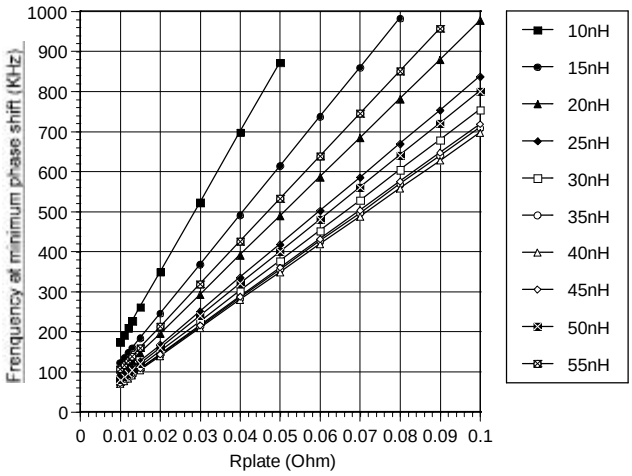


Figure 4.2 The frequency at the minimum phase shift vs. the target plate resistance for diverse fixed values of the target plate inductance. The input stage is an ideal voltage controlled current source.

For a specific L_{plate}, which is extracted from the minimum phase shift readout via Figure 4.1, R_{plate} can be derived from the frequency at which the minimum phase shift occurs by referring to Figure 4.2. The sensitivity of the frequency at which the minimum phase shift occurs to R_{plate} ranges from 69.6 to 174 KHz /0.01Ω, and the linearity is within 700Hz for each fixed value of L_{plate}.

4.2 RESOLUTION OF THE MAIN CIRCUIT

The resolution is defined as the minimum detectable change in the measurand that can cause a change in the output signal [12]. According to this definition, the resolution of the circuit configuration discussed in the previous section is extremely small. However, it is impossible to obtain the phase shift directly and to build an ideal voltage-controlled current source. Thus, to evaluate the resolution of the practical sensing system before any feedback is involved, the main circuit shown in Figure 3.11 is simulated through the a.c. analysis. The result is given in Figure 4.3. Due to the fact that the output impedance of the transconductance amplifier is not infinite, the minimum phase shift changes with the target plate resistance for a fixed target plate inductance and this change can be as high as 0.8 degree. Because the magnitude of this change is not random but depends on other known parameters, this undesirable result can be minimized by modifying the minimum phase shift at the output Φ to Φ' through the following equation,

$$\Phi' = \Phi + A \times \left(\frac{f - f_o}{k} \right) + \Delta\Phi' , \qquad (4\text{-}1)$$

where f is the frequency readout at which the minimum phase shift occurs and

the coefficients and constant are listed in Table 4.1. The variation of the minimum phase shift due to the change of R_{plate} for a fixed L_{plate} is thus below 0.03 degree as listed in the ' Φ′ error ' in Table 4.1. The resolution of L_{plate} is also shown in the table and has a maximum value of 0.04nH.

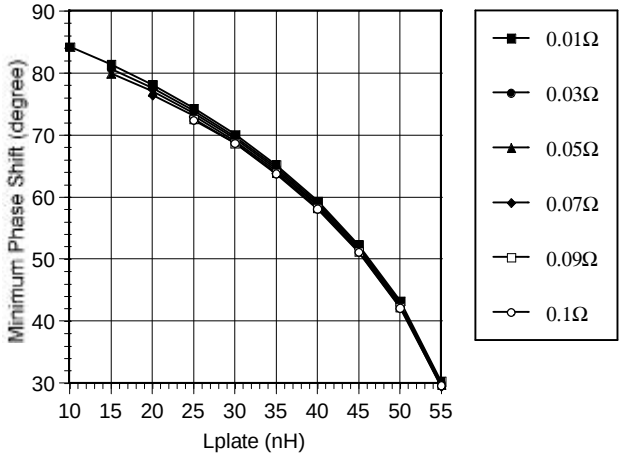


Figure 4.3 The simulation results of the main circuit: the minimum phase shift vs. the target plate inductance for diverse fixed target plate resistance.

i	Φ (degree)	k (KHz/Ω)	A(degree/Ω)	f_o (KHz)	ΔΦ'(degree)	Φ' error (degree)	Lplate Resolution (nH)_
2	≥82	214	0.209	181	0.193	0.011	0.02
3	79~82	140	0.137	125	0.13	0.02	0.03
4	76~79	106	0.103	99	0.099	0.01	0.01
5	72~76	88	0.08	84	0.082	0.03	0.04
6	67~72	78	0.709	75.5	0.07	0.005	0.005
7	62~67	73	0.0626	71	0.124	0.01	0.009
8	56~62	71	0.057	70	0.057	0.01	0.007
9	49~56	73	0.0538	72	0.055	0.002	0.001
10	37~49	81	0.0535	80	0.054	0.003	0.001
11	≤37	109	0.0616	107	0.061	0.002	0.001

Table 4.1 Adjustment parameters for the minimum phase sift readout of the main circuit. *A* is the slope of the minimum phase shift vs. R_{plate} for each L_{plate} of i×5nH, *k* is the slope in Figure 4.2 for each L_{plate} of i×5nH, f_o is the frequency at which the minimum phase shift happens for each L_{plate} of i×5nH and R_{plate}=0.01Ω, and *DF ¢*is the fitting constant. *F ¢ error* is the magnitude of the maximum variation of Φ′ caused by the change in R_{plate} for each fixed L_{plate} of i×5nH. L_{plate} resolution is derived from dividing*F ¢error* by the differential of the curve in Figure 4.1 at each L_{plate} of i×5nH.

So far, it is supposed that the transconductance amplifier is a linear device so that the small signal model used here is valid. However, the input signal of the transconductance amplifier has an amplitude of 0.2Volt for the purpose of providing a large current at the output and enhancing the power efficiency. With this large signal of 0.2Volt, the nonlinear effect of the transconductance amplifier must be taken into account. The method used to evaluate the degradation of resolution caused by the nonlinear effect is illustrated in Figure 4.4. With -0.2Volt and +0.2Volt as the input offset voltage, the a.c. performance deviates from the expected performance with the ideal input offset voltage of 0V. The magnitudes of the deviation, which depend on the values of R_{plate} and L_{plate} and can be taken as the minimum detectable changes in the phase ($\Delta\Phi$) and the minimum effective changes in the frequency (Δf), respectively, are shown in Table 4.2 as well as the resolution of R_{plate} and L_{plate} if only the nonlinear effect is considered. Three values of R_{plate} are chosen to test three different frequency ranges, and for each R_{plate}, two values of L_{plate}, one of which corresponds to the sharpest phase response (low F) and the other relates to the smoothest one (high Φ), are applied. We observed that the resolution degrades with higher R_{plate} and lower L_{plate}, i.e., higher frequencies and smoother phase response.

It is important to bias the output of the transconductance amplifier at zero Volt, otherwise there will be a d.c. current flowing through the primary coil, the magnitude of which will be sensitive to the variation of the coil resistance. As a

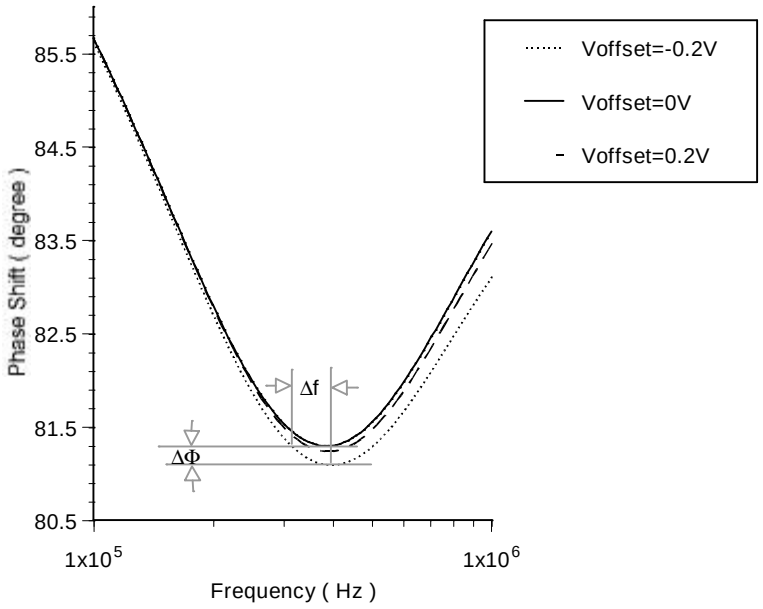


Figure 4.4 Illustration of the nonlinear effect of the transconductance amplifier. R_{plate} = 0.03Ω and L_{plate} = 15nH.

R_{plate} (Ω)	**0.01** (Low Freq. 50KHz~120KHz)		**0.03** (Middle freq. 120KHz~600KHz)		**0.1** (High Freq. 600KHz~1MHz)	
L_{plate} (nH)	**50** (low Φ)	**20** (high Φ)	**55** (low Φ)	**15** (high Φ)	**50** (low Φ)	**30** (high Φ)
DF (degree)	0.01	0.02	0.034	0.07	0.1	0.13
DL_{plate} (nH)	0.004	0.03	0.013	0.1	0.04	0.11
Df (Hz)	2K	6K	17K	60K	72K	104K
DR_{plate} (Ω)	3E-4	6E-4	2E-3	4E-3	9E-3	1.3E-2
d	0.025	0.053	0.06	0.16	0.089	0.13

Table 4.2 Minimum detectable changes in phase shift (*DF*) and minimum effective changes in frequency (*Df*) of the main circuit due to nonlinear effects of the transconductance amplifier. The resolutions of L_{plate} (DL_{plate}) and R_{plate} (DR_{plate}) are then derived from dividing *DF* and *Df* by the differential of the curve in Figure 4.1 and *k* at the specified L_{plate} and R_{plate}, respectively. Coefficient *d* is calculated by Eq. (4-2).

result, the variation of the coil resistance will change the d.c. biasing condition of the transconductance amplifier and thus cause deviation in the a.c. performance.

The phase detector and the FVC do not influence the a.c. performance, but the ripples at the d.c. output of the integrator restrict the resolution. The amplitude of the ripples is 0.1mV, which can be converted to 0.0073° and 45Hz via the transfer functions of the phase detector and the FVC, respectively.

Summing up the effects drawn by the three sources causing the degradation of the resolution, the finite output impedance and the nonlinear effect of the transconductance amplifier, and the ripple at the integrator output, it is evident that the resolution of the main circuit is dominated by the nonlinear effect of the transconductance amplifier.

4.3 COMPARISON BETWEEN THE SUCCESSIVE AND THE ITERATIVE FEEDBACK SCHEMES

4.3.1 Performance of the Successive Feedback

In Section 3.3, the coefficient which determines the frequency step, δ, was not quantified. Now, since the minimum effective changes of the frequency have been obtained by the simulation of the main circuit, δ can be given in Table 4.2 by applying

$$\delta = \frac{\Delta f}{f}, \tag{4-2}$$

where *Df* is as listed in Table 4.2 and *f* is the frequency at which the minimum phase shift occurs for the specified L_{plate} and R_{plate}. It is observed that the smoother the phase response to frequency is, the larger δ is. Since the smoother phase response to frequency corresponds to the longer distance between the sensor and

the metal target, it is clear that there is a tradeoff between the resolution of the detection for the shorter distance and the maximum detectable proximity if a fixed δ value is chosen.

R_{plate} (Ω)	**0.01** (Low Freq. 50KHz~120KHz)		**0.03** (Middle freq. 120KHz~600KHz)		**0.1** (High Freq. 600KHz~1MHz)		Simulation method
L_{plate} (nH)	**50** (low Φ)	**20** (high Φ)	**55** (low Φ)	**15** (high Φ)	**50** (low Φ)	**30** (high Φ)	
Φ of Sensor with Ideal Input Stage (Section 4.1)	43.388°	78.321°	30.453°	81.691°	43.388°	70.255°	a.c. analysis
Φ of Main Circuit †† (Section 4.2)	43.388°	78.321°	30.453°	81.68°	43.389°	70.257°	a.c. analysis
Accuracy of Φ of Successive Feedback Scheme	0.73%	-1.5%	1.0%	*	2.6%	*	transient analysis
Accuracy of Φ of Iterative Feedback Scheme	-0.79%	-5.6%	0.30%	1.8%	0.89%	-3.6%	transient analysis
Resolution of L_{plate} with Iterative Feedback Scheme (nH) †	0.06	0.1	0.04	0.1	0.07	0.1	transient analysis

Table 4.3 Comparison of the accuracy of phase readouts of the successive and iterative feedback schemes, where 85° is taken as the full-scale output signal. Φ is the minimum phase readout. * The circuit could not sense a change in the polarity of the slope of the phase response to the frequency in the scanning frequency range. †A refined VCO with the level one model applied is used here. ††The phase readings shown have been converted to Φ′ by Eq. (4-1).

Letting δ be fixed to 0.025, the desired δ value for L_{plate} = 50nH and R_{plate} = 0.01Ω, in the circuit shown in Figure 3.11, the successive feedback circuit is simulated for the six conditions given in Table 4.2 through transient analysis. Table 4.3 and Table 4.4 list the accuracy of the phase and frequency outputs. Due to the

nonlinear characteristic of the VCO and the voltage level translator, the average effective magnitudes of δ are 0.025, 0.05 and 0.075 in the three frequency ranges concerned, respectively, and are very close to the desirable values of δ for lower Φ in Table 4.2. Therefore, the accuracy for lower Φ is within 2% while the change of the polarity of the slope of the phase response to the frequency may never be sensed in the scanning frequency range for higher Φ.

R_{plate} (Ω)	**0.01** (Low Freq. 50KHz~120KHz)		**0.03** (Middle freq. 120KHz~600KHz)		**0.1** (High Freq. 600KHz~1MHz)		Simulation method
L_{plate} (nH)	**50** (low Φ)	**20** (high Φ)	**55** (low Φ)	**15** (high Φ)	**50** (low Φ)	**30** (high Φ)	
f of Sensor with Ideal Input Stage (Hz) (Section 4.1)	80K	98K	319K	368K	800K	754K	a.c. analysis
f of Main Circuit (Hz) (Section 4.2)	80K	99K	321K	386K	812K	780K	a.c. analysis
Accuracy of ***f*** of Successive Feedback Scheme	1.3%	1.4%	1.1%	*	-2.7%	*	transient analysis
Accuracy of ***f*** of Iterative Feedback Scheme	0%	-4.9%	1.0%	-25%	-18%	-22%	transient analysis
Variation of ***f*** of Iterative Feedback Scheme	±2K	±4K	±18K	±7K	±15K	±30K	transient analysis
Resolution of R_{plate} with Iterative Feedback Scheme (Ω) †	1.2E-3	4.8E-3	2.5E-3	2.9E-3	8.9E-3	9.0E-3	transient analysis

Table 4.4 Comparison of the accuracy of the frequency readouts of the successive and iterative feedback schemes, where 1MHz is taken as the full-scale output signal. *f* is the frequency readout. * The circuit could not sense a change in the polarity of the slope of the phase response to the frequency in the scanning frequency range. †A refined VCO with the level one model applied is used here.

4.3.2 Performance of the Iterative Feedback

δ is desirable as a variable rather than as a constant in order to avoid the tradeoff described in the previous section. Eq. (3-14) and Eq. (3-15) are thus applied to determine the frequency steps. The accuracy of the iterative feedback circuit is shown in Table 4.3 and Table 4.4 to compare with that of the successive feedback scheme. Due to the 1mV decay at the outputs of the sample-and-hold circuits during a clock cycle, there is a ±0.5mV variation at each phase readout, which is 0.037° after being converted by the transfer function of the phase detector. This is the reason why the operation frequency still varies after convergence is achieved. The frequency variations observed are listed in Table 4.4 and are generally lower than the minimum effective frequency steps in Table 4.1, so this phenomena can be ignored. But the ±0.5mV variation at the phase readings restricts the resolution of L_{plate}.

The iterative scheme is capable of extracting a smoother phase response and generating a generally lower error compared to the successive scheme. But the accuracy in the frequency output is still unsatisfactory for higher Φ because the circuit converges at a much lower frequency than the desired value. Since the phase response to the frequency is quite flat for higher Φ, the accuracy of the phase reading does not reflect this phenomenon. One of the possible factors contributing to this problem is the high THD of the sinusoidal signal at the output of the sine-shaping circuit, which is frequency-dependent and, in turn, causes the phase detector to be sensitive not only to the phase shift but also to the operating

frequency. Hence, a decrease in the phase shift due to an increase in the operating frequency may be reflected as an increase at the phase detector output. Even though a good sine-shaping circuit can be built by using the 0.8μm CMOS model, the serious channel length modulation effect of the model limits the performance of the VCO. Referring to the VCO configuration illustrated in Figure 3.1, the channel length modulation effect destroys the equivalence among i_1, i_2 and i_3 and also makes the sourcing and sinking currents of the VCO capacitor, i_2 and i_3, vary with the output voltage (V_{out}). In the time domain, the varying current results in a nonlinear increase or decrease of the output voltage, while the unequal sourcing and sinking currents generate asymmetric output waveforms. These phenomena are reflected in the form of higher order harmonics in the Fourier series representation of the output waveform of the sine-shaping circuit, which are then amplified by the transformer with a gain higher than that for the fundamental harmonic.

Another possible reason for the unsatisfactory accuracy is that the amplitude of the desired signals at the secondary coil is so low (several millivolts) that a significant error can be generated by the offset voltage of the comparator in the phase detector. Thus an amplifier should to be added between the secondary coil and the comparator, while another amplifier of the same design should also be put before the other comparator in the phase detector to avoid any phase error produced by the amplifiers.

If a simple level one model with very low channel-length modulation parameters ($\lambda_p = \lambda_n = 0.005$) is applied to the transistors in the VCO and two

amplifiers are added in the phase detector, the accuracy of the frequency and the phase can be improved to be below 8% and 0.6%, respectively, for all the high Φ conditions specified in Table 4.3 and Table 4.4. The resolution of the refined interface circuitry is also listed in the tables and is approximately of the same order as that shown in Table 4.2. Therefore, it can be concluded that the nonlinear transfer function of the transconductance amplifier dominates the resolution.

The iterative feedback scheme is also superior to the successive one with respect to sensor response time. The total number of clock cycles needed for the successive feedback scheme to sense the minimum phase shift is proportional to the frequency output and can be as high as fifty, compared with that of the iterative feedback scheme which has an average of fifteen and does not depend on the frequency output.

4.4 EFFECT OF VARIATION IN COIL RESISTANCE

Although the a.c. analysis of the two-coil sensing element has been shown to be unchanged as the coil resistance increases, the sensor system is inclined to lose sensing capability for coil resistance higher than 1Ω when the transient analysis is performed in the interface circuit. This is a result of the output voltage swing of the transconductance amplifier being higher than the range in which the linear transfer function can be held if the coil resistance increases above 1Ω and the output current is still kept higher than 200mA to excite the eddy current in the target plate. For the higher coil resistance, say 200Ω, the reason for the loss of sensitivity is simply that the output voltage swing exceeds the power supply voltage. Therefore, we have shown that the circuit discussed is immune to process

deviations, which cause a resistance variation of several tens of percentage points, but the circuit would require some redesign if it were to be used with a scaled sensor having much higher resistance.

Chapter 5: Summary and Conclusion

An interface circuit for the two-coil proximity sensor has been designed and simulated using the 0.8μm CMOS model available through the MOSIS service. Except for several bipolar transistors, which can be fabricated on the same chip if a BiCMOS process is available, the whole circuit with the sensing element can be integrated monolithically by the conventional CMOS process. The periodic signal driving the primary coil is generated by an on-chip VCO and conditioned by a transconductance amplifier. For the output stage, a phase detector and a FVC extract the phase shift and the operation frequency, respectively, in the forms of d.c. voltage. Feedback schemes are applied to make the operation frequency converge to the value at which the minimum phase shift happens. The two measurands, L_{plate} and R_{plate}, can thus be determined by the two d.c. voltage output readings representing the minimum phase shift and the operation frequency at which the minimum phase shift occurs, respectively. It is observed that the accuracy can be significantly enhanced by applying the iterative feedback scheme. However, the transformer structure of the sensing element amplifies the undesirable higher order harmonics in the Fourier series representation of the input signal so that the sinusoidal output signal is seriously distorted. The configuration of the sinusoidal VCO needs to be refined or a feedback-controlled tunable bandpass filter has to be added to the output stage to reduce this problem.

Another main factor degrading the resolution and accuracy of the circuitry is the nonlinear effect caused by the transconductance amplifier as mentioned in Section 4.2. Further investigations are necessary to avoid the tradeoff between the linearity of the transfer function and the power efficiency of the transconductance amplifier.

An alternative way to more accurately evaluate the frequency step in the iterative feedback loop is to convert the analog signals at the outputs of the FVC and the phase detector into the digital domain by means of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). The analog computer described in Chapter 4 will be replaced by digital programming circuits, and hence the nonlinear effect and offset voltage of the analog computing components, such as the multifunction converters and difference amplifiers, for example, can be eliminated.

The characteristic of the proximity sensor makes it possible to measure the distance independent of the conductivity of the target material. The conductivity of the target can also be identified by using multiple output readings. Further work needs to be done to quantify the relationship between the two measurands, L_{plate} and R_{plate}, and the two physical parameters, distance and conductivity of the target plate.

A planar sensing element based on micromachining technology has been fabricated with a mask design similar to the one described in Figure 2.9 [27]. The silicon substrate underneath the transformer consisting of two inductors was removed to eliminate the effect drawn by the parasitic capacitance and the resistive

loss. The coil resistance and inductance are 5.5Ω and 10nH, respectively. Based on an approximate and reasonable assumption for scaling down the geometrical dimension of the coils, the resistance of the target plate (R_{plate}) is scaled up and the inductance of the target plate (L_{plate}) is scaled down proportionally to the scale factor, if the target distance is scaled down as well. The coupling factor between the two coils remains the same [8]. The a.c. analysis of the sensor model in Figure 2.10 with the parameters specified above shows that the characteristic of the phase response to the frequency remains approximately the same except that the operation frequency range increases by the inverse square of the scale factor. Therefore, the interface circuit can be applied to the micromachining sensor if the transconductance amplifier is modified to provide more power and to keep zero phase shift between the output current and input voltage. Also, the operation frequency range of the FVC and the VCO needs to be enhanced by the inverse square of the scale factor.

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