Chapter 6

Conclusion

In this dissertation an efficient methodology has been presented for extracting parameters of high speed digital interconnects. First, a single distributed circuit with frequency dependent circuit elements has been developed for microstrip lines on lossy substrates. These kind of structures are common in interconnect structures over silicon substrates. The distributed circuit provides fast and accurate solutions and the results are in good agreement with computationally expensive full-wave calculations. The same methodology applied to lossy substrates above, was then extended to conductor loss calculations in two dimensional structures. Geometrically dividing conductors into sections and calculating an effective internal impedance for each section has been shown to be a fast and accurate technique for representing frequency dependent behavior of conductors at their surfaces. Analytically obtaining skin effect as oppose to numerical evaluation accelerates computation time and saves memory. Coupled to an external solver, the effective internal impedance approach is very efficient for extracting series impedance in high speed digital interconnect structures.

The effective internal impedance approach has also been coupled to two external field solution techniques. The first, conformal mapping, is a well established technique used for quasi-static analysis. Using the scaling property

of conformal mapping, an integral expression has been derived for series impedance, which has been evaluated with 24-point Gaussian Quadrature at each frequency point. Although the series impedance extraction is very fast with conformal mapping, the set of geometries that this methodology is applicable to is limited. A more general approach using a modified current filament technique has been presented that profits from the speed gain that effective internal impedance provides. The so-called "Surface Ribbon Technique" couples the effective internal impedance approach with the filament technique. The interactions between conductors (the proximity effect) have been captured by the mutual inductances between ribbons on the surface and the internal behavior (the skin effect) has been modeled by the effective internal impedance assigned to each ribbon.

After the extraction, to obtain performance limiting parameters such as crosstalk and delay, simulation has to be done in time domain. The extracted frequency dependent parameters must be represented in the time domain efficiently. One solution is to synthesize a circuit from extracted parameters. For two dimensional interconnect structures this can be done by a suitable lumping algorithm. The surface ribbon technique provides a good basis to obtain a circuit model for a given interconnect structure: each ribbon can be represented by an inductance plus an RL ladder to capture dc resistance and skin effect, and mutuals between inductances can be used to capture proximity effects.

A major part of the interconnect structures at the board and chip level are three dimensional, which means the length of the structure is comparable to its width. Using three dimensional inductance calculations, the surface ribbon technique can be used to extract three dimensional interconnect structures.

A more rigorous approach is to include the effect of bends in the calculation. This would require a new definition of effective internal impedance for three dimensional structures. The external effects would be modeled by the mutual interaction of surface patches. Another problem facing geometrical extraction is capacitance. For two dimensional interconnect structures embedded in uniform dielectric the capacitance matrix can be calculated by inverting the inductance matrix obtained from the surface ribbon technique by setting the effective internal impedance to zero.

As the complexity and speed of integrated systems increase, designers need CAD tools that are faster and more accurate to handle larger number of circuits and tighter error margins. The effective internal impedance approach coupled to the surface ribbon technique provides a fast and accurate series impedance extraction suitable for use in CAD tools.