Chapter 1

Introduction

With increasing speed and complexity of integrated circuits, the microprocessor industry has been the driving force of VLSI technology. Wide usage of personal computers and workstations makes microprocessor industry a very profitable business. In todays ever expanding market, companies are competing to be the first to introduce the fastest chip. To make the fastest chip not only requires a leading edge in process technology but also in the understanding of device physics and knowledge of electromagnetics. As the minimum feature size shrinks active devices gain speed and interconnect parasitics become dominant in delay and signal integrity calculations. Decreasing feature sizes have increased chip sizes, complexity at ever higher speed; as a result the number of the pins coming out of a chip have increased considerably, first to communicate information faster and second for the necessity of having close returns to signal lines to reduce inductance.

The trend of increasing speed and reduction in size has affected the next stage of integration, namely multichip modules and printed circuit boards. High pin count has required in high density interconnect structures at the board level thus increasing the need for accurately predicting delay and crosstalk. For high speed digital signal propagation interconnections on multichip modules

and circuit boards should be modeled as transmission lines[2]. In the delay and crosstalk calculations the first step is to extract parameters from the geometrical information defined by layout. Then a circuit simulator uses the parameters to calculate the delay and crosstalk. In most of the cases the parameters extracted are in the frequency domain, but required results, the delay and crosstalk, are in the time domain. Common ways of representing frequency domain parameters in the time domain are lumping of the distributed circuit[42, 10] or convolution of the transfer function[23, 5, 11]. In that sense, for their ease of use in lumping or convolution, the most useful parameters are series impedance and shunt admittance.

In this dissertation an accurate and fast extraction technique for the series impedance of high speed digital interconnects is presented. The series impedance is a function of frequency and consists of a resistive and an inductive part. The parameters extracted should accurately model the resistance and inductance in the frequency band of interest[1].

Due to cost effectiveness and compatibility of process technology silicon-on-silicon multichip modules are commonplace. Ease of manufacturing small line widths with this technology makes production of high density interconnects possible. In some cases the interconnects on silicon are isolated from the substrate by a silicon dioxide layer. These kind of structures are also called Metal-Insulator-Silicon (MIS) microstrip lines. Having the return on the opposite side of the semi-conductive substrate ($\sigma \approx 100$ $(\Omega\text{cm})^{-1}$) this structure can support three distinct modes of wave propagation. The quasi-TEM and

[1]The maximum frequency is calculated from the rise time as $f_{max} = n/t_r$, where t_r is the rise time and n is usually equal to 1 or 2.

slow-wave modes were modeled using a distributed circuit before[14]. In the second chapter of this dissertation a distributed circuit will be derived to model all three modes[2]. The circuit has a frequency dependent series impedance in the series arm, and the same circuit proposed in [14] in the shunt arm. The series impedance is calculated through a function depending on the frequency, substrate conductivity and geometry of the structure.

In Chapter Three, a similar method to the one used to obtain the series impedance in MIS lines will be applied to calculate an effective internal impedance for rectangular metal bars. The effective internal impedance represents the contribution from the inside of conductors to the series impedance. Using this approach internals of conductors can be removed from the problem and replaced with an impedance shell. The effective internal impedance should model behavior of a conductor over a wide frequency band, from dc to the frequency determined by the rise time of the digital signal that is propagating through the conductor. In this chapter, a number of rules will be developed to calculate the effective internal impedance of a given conductor geometry. The validity of the approach will be investigated.

The conformal mapping technique is a very well established method for solving two dimensional quasi-static problems with rectangular cross sections. In Chapter Four, utilizing the effective internal impedance technique, conformal mapping will be used to calculate the resistance and inductance of transmission lines from dc to high frequencies. The application of conformal mapping to calculate the loss (hence the resistance) has been shown at high frequen-

[2]The three modes supported by a MIS microstrip line are the slow-wave, quasi-TEM, and skin-effect modes.

cies where skin depth is much smaller than the transverse dimensions of the conductors[7, 30]. At lower frequencies calculation of series impedance using conformal mapping was not possible. In this chapter, by utilizing the effective internal impedance concept, a single model will be used to calculate the resistance and inductance over the full frequency range. Using a single model provides a smoother transition from dc to high frequency behavior and simplifies the calculation. The results of the calculations will be compared to measured values for a number of test structures.

A special map, the Schwartz-Christoffel map, is suitable for mapping interconnect structures. This map can transform rectangular conductor traces into parallel plates. The most important drawback of the Schwartz-Christoffel map is the difficulty of finding the map. The map parameters are found by solving a number of non-linear equations simultaneously. The number of equations are determined by the number of corners in the cross section and symmetry. For multi-conductor transmission lines, conformal mapping can loose its advantage of being fast because of the complexity of solving these equations.

In Chapter Five, a modified filament technique that removes the internals of conductors from the calculation by means of an effective internal impedance concept will be introduced. The filament technique introduced by Weeks *et. al.*[39] is a convenient way of extracting series impedance for multi-conductor lines. At high frequencies where the skin depth is smaller than the size of conductors the filament technique becomes slow and generates massive matrices. A way around this problem is to use the effective internal impedance concept and model the skin-effect through an analytic function instead of capturing it by sampling current distribution with filaments. In such a "ribbon"

technique, as with the modified conformal mapping technique, the conductors will be replaced with an effective internal impedance shell. The internal electromagnetic behavior of the conductors will be modeled with the effective internal impedance function assigned to each surface ribbon and external behavior will be obtained from the interaction of ribbons with each other. To show the efficiency of the technique the results will be compared to the full Weeks filament technique for computation time and to measured data for accuracy.