CHAPTER 4 : FABRICATION ISSUES

A schematic diagram of the prototype proximity sensor is shown in Fig. (4-1). A two-coil transformer is fabricated in an etched hole through a silicon wafer, on a Si_3N_4/SiO_2/Si_3N_4 membrane. Interconnects are placed along the walls of the hole. The sense and drive circuitry is placed on the back of the wafer.

A Si_3N_4/SiO_2/Si_3N_4 stack is deposited using LPCVD (low pressure chemical vapor deposition) on a two side polished <100> wafer. On the front side, the dielectric stack forms the membrane material while on the back the same stack acts as a mask when the silicon bulk-etching step is performed. A hole is etched in the Si_3N_4/SiO_2/Si_3N_4 stack on the back of the silicon wafer using reactive ion etching. Next the silicon is bulk micro-machined (etched) using KOH leaving a Si_3N_4/SiO_2/Si_3N_4 membrane in the front of the wafer supported by a pyramidal hole. The pyramidal hole is formed due to the anisotropic etching of the KOH along the <111> planes of the wafer. The coils are then patterned on the back of the membrane. This is done to protect the coils from the lubricant (as discussed in Chapter 1). The more important reason, however, is that silicon, as a semiconductor, acts as a 'virtual plate' in close proximity to the two coils affecting their performance as transducers [1]. By removing this silicon, the Q-factor of the coils and their performance is greatly enhanced.

Fig. (4-2) shows a schematic of the two-coil transformer fabricated in an etched hole. The figure shows patterned interconnects along the side-wall of the hole. Also, since the spiral coil needs a bridge to connect the center of the coils to the interconnects, two levels of metal separated by an inter-metal dielectric are needed.

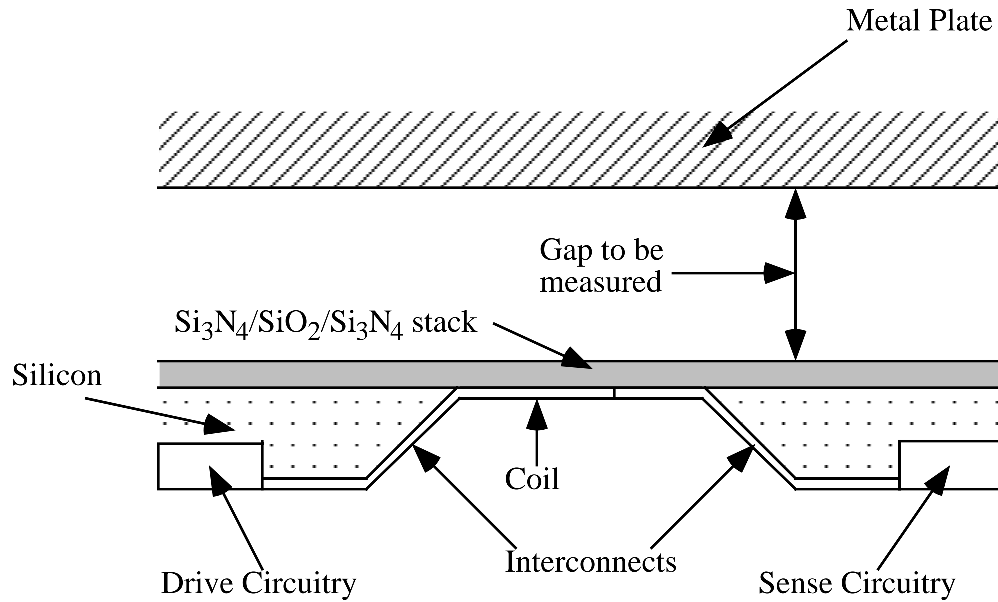


Fig. (4-1): Schematic diagram of the proximity sensor.

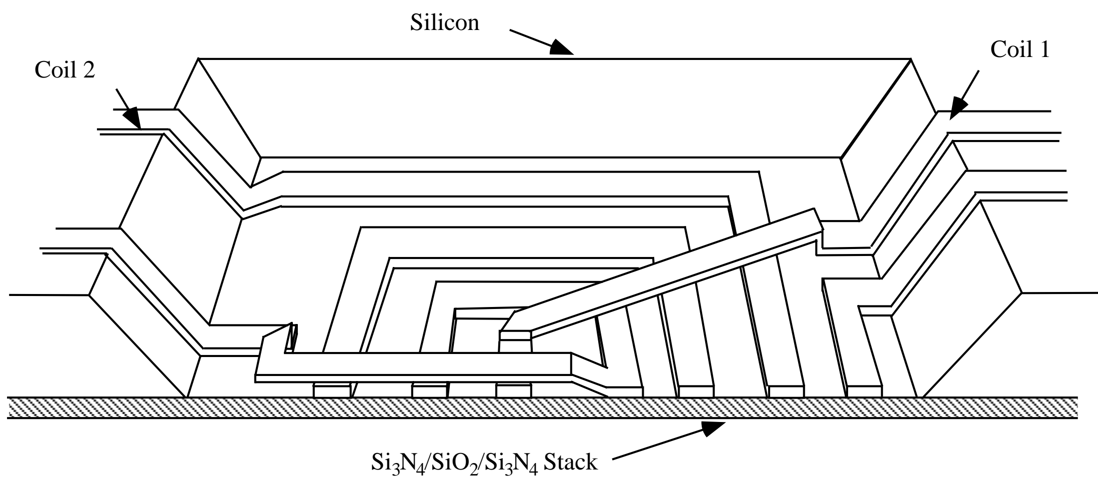


Fig. (4-2): Schematic of the two-coil transformer.

4.1.0 The Membrane

Membranes made of deposited silicon dioxide only tend to buckle since they have an in-built compressive stress [2]. On the other hand membranes made of silicon nitride have an in-built tensile stress which causes them to stretch flat over the etched hole. A composite membrane ($Si_3N_4/SiO_2/Si_3N_4$ membrane) was used in this case in order to obtain a stress compensated membrane. This was required because in the fabrication of the pressure sensors (discussed in Chapter 1), holes are made through the membrane. In the case of the silicon-nitride membranes, this would cause the membranes to crack due to the stress concentration produced by the holes in the membrane.

Potassium hydroxide (KOH) [3] is used as the silicon etchant since it produces more reproducible and controllable results compared to ethylene diamine pyrocatechol (EDP) [4]. Also, KOH etches more uniformly than EDP. Due to this the stress produced in the membrane as it is about to be released from the silicon is reduced and is uniform across the membrane, decreasing the tendency of the membrane to crack. EDP produces hillocks of silicon towards the end of the bulk etch step. This produces concentration of stress in these regions of the membrane causing it to crack.

KOH attacks silicon dioxide and hence silicon dioxide cannot be used as an effective mask on the back of the wafer. This is another reason why a composite membrane was chosen.

4.2.0 The Overhang Problem

Initially it was thought that a circular mask hole to etch off the masking dielectric on the back of the wafer could be used. This would eliminate the need to perform any alignment to the crystal axes of the wafer. However a circular hole in the dielectric produces a hole in the silicon with a rectangular base bounded by the <111> planes in

the silicon as shown in Fig. (4-3). This means there is a large amount of undercut under the masking dielectric producing large overhangs of the dielectric. These overhangs prevent a uniform coating of the hole with photoresist. To eliminate the overhangs a square hole mask was made and aligned to the flat of the wafer (to align it to the crystal axes).

In Fig. (4-3) we can see the overhangs which have in fact broken in the upper left and right corners of the hole since the overhangs are not supported by the silicon. The hole in the silicon is a pyramidal hole with a square base which forms a boundary of the circular hole in the dielectric. Also the membrane formed in the front of the wafer is out of focus in the picture since it is 300 µm below the level of the masking dielectric.

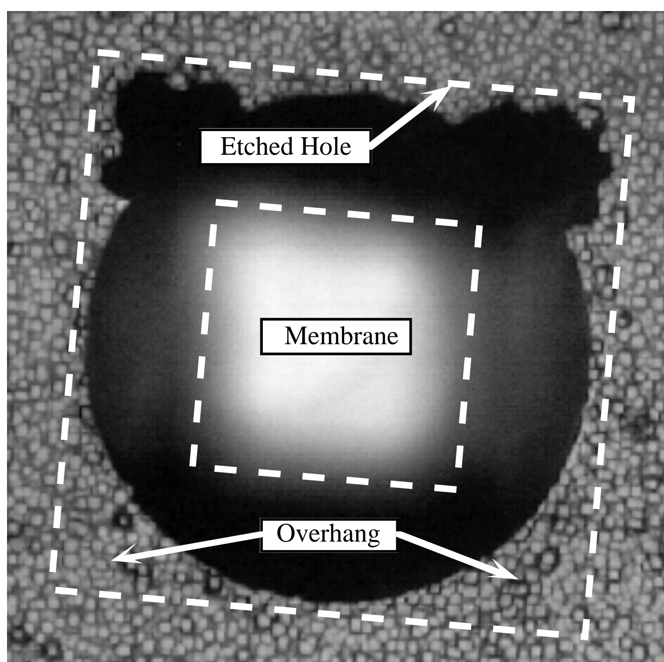


Fig. (4-3): Overhang produced due to the circular mask hole used to etch the masking dielectric on the back of the wafer.

4.3.0 Photoresist Profiles

As can be seen from Fig. (4-2), the coils are placed inside the etched hole on the back of the membrane. Contacts to the coils are placed along the walls of the etched hole. This means that photolithography needs to be performed inside the hole and along the walls of the etched hole. In order to perform photolithography it is important to get a uniform and conformal coating of photoresist along the walls of the hole, along the membrane and the top and bottom edges of the hole.

An interesting aspect of spinning the photoresist into an etched hole is shown in Fig. (4-4) and Fig. (4-5). In both the cases PR 5214E was spun on the samples at 3000 rpm. Fig. (4-4) shows the top view of the photoresist in a hole of a sample which had two etched holes and was rectangular in shape. This is an accumulation of photoresist along the edge of the hole further away from the axis of spin, shown by a black dot. There is also a slight thinning of the photoresist close to the region of accumulation. This has resulted in the loss of the coil pattern in these regions.

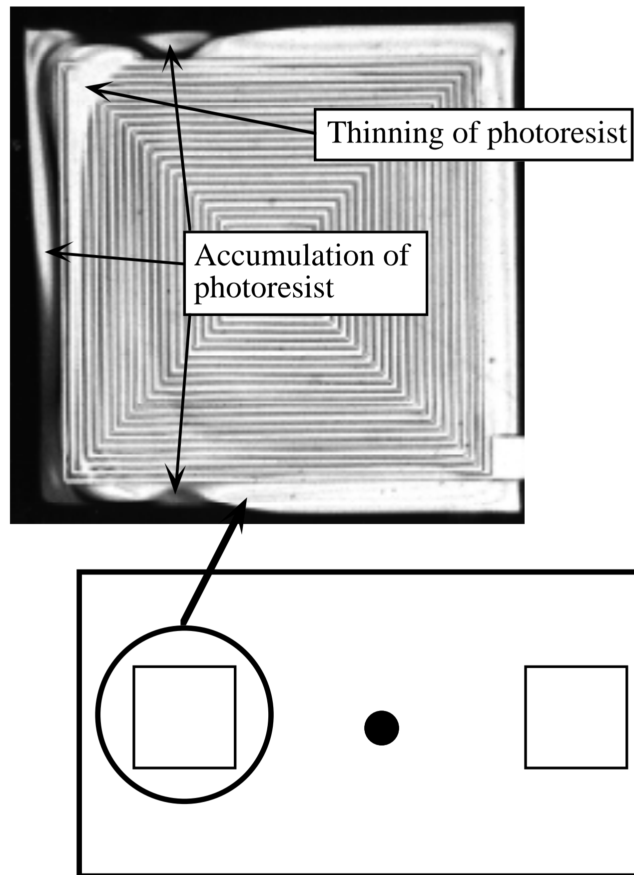


Fig. (4-4): Top view of the photoresist spun on a sample with two holes.

Fig. (4-5) shows the top view of the photoresist in a hole of a sample which had four holes and was more square shaped. Accumulation of photoresist has occurred again but this time it is at a corner which is again away from the axis of spin. There is almost no thinning of the photoresist.

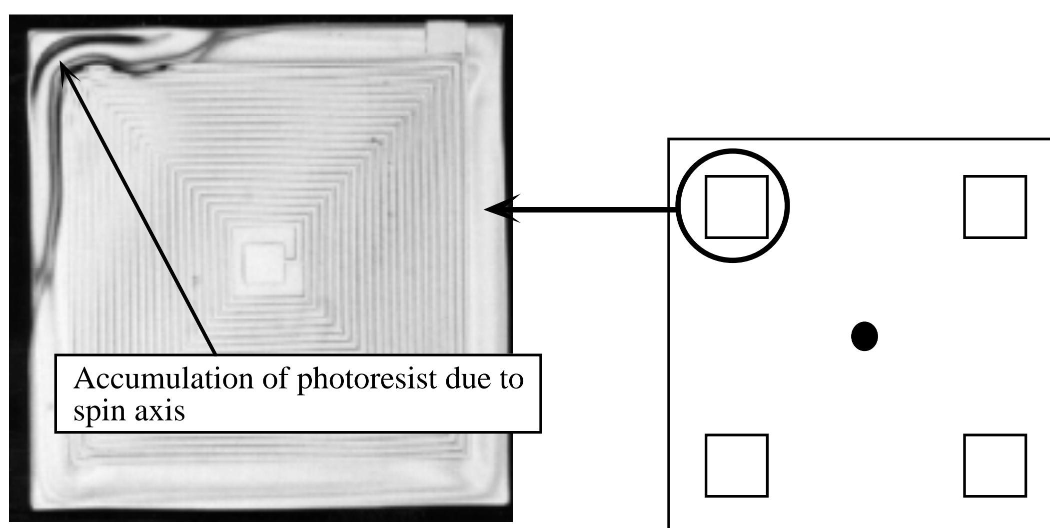


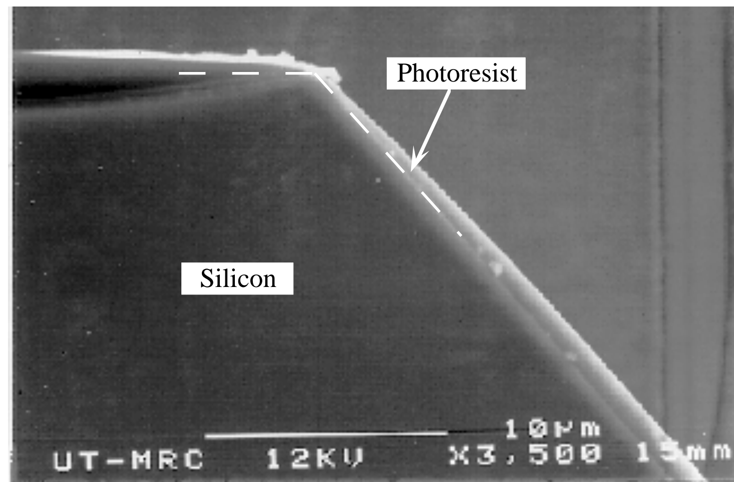
Fig. (4-5): Top view of the photoresist spun on a sample with four holes.

In both the cases the region of accumulation decreased in size with an increase in the spinning speed. The thinning in the two hole sample, however, continued to persist. Thus the four hole sample was used to obtain a more uniform coating of photoresist.

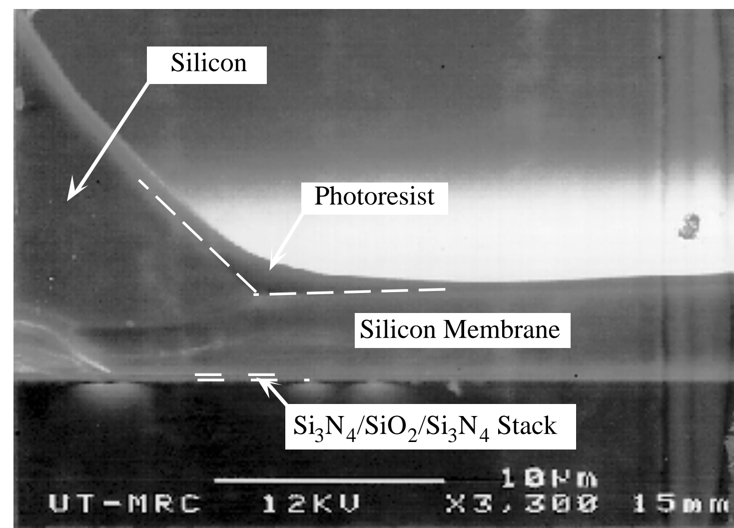
Shown in Fig. (4-6) are the resist profiles along the top edge and bottom edge of an etched hole in the four hole configuration. As can be seen from the profiles, the photoresist is approximately 1 µm thick and quite conformal. There is a slight thinning of the photoresist along the top edge and a slight thickening along the bottom edge. How-

ever along the walls and at the membrane, the coating of the photoresist is very uniform. Note that the SEM of the profile along the bottom edge of the hole shows a silicon “membrane”. This means that the silicon, in this case, was not etched off completely (up to the dielectric membrane). This was done so that the sample could be cleaved along the middle of the hole without breaking the bottom membrane.

The top view of a hole of a four hole sample coated with PR 5214 E and spun at 4000 rpm is shown in Fig. (4-7). There is a slight accumulation at the upper right hand corner leaving almost the entire membrane coated with a relatively uniform coating of photoresist. A pattern of a single coil has been exposed in the photoresist using techniques discussed in section 4.4.0. The spiral coil has 20 turns with a line width of 10 μm at 10 μm intervals. The coil occupies an area of 1 mm by 1 mm.



(a)



(b)

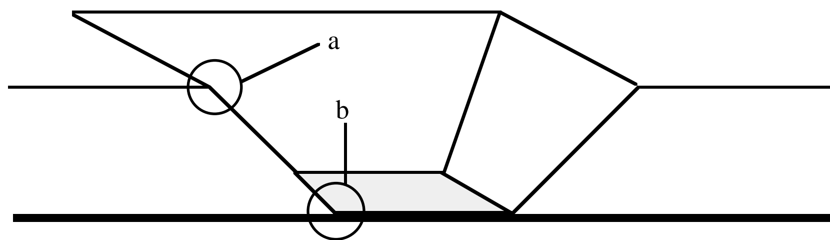


Fig. (4-6): Photoresist profiles inside the etched hole of a four hole sample.

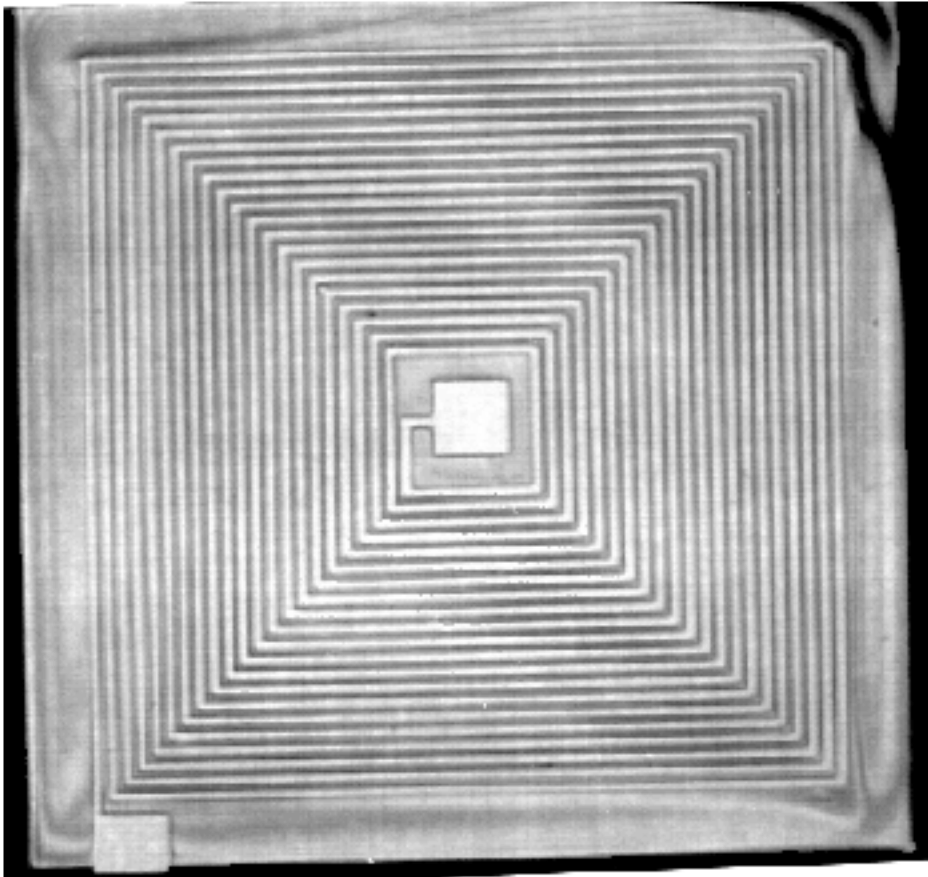


Fig. (4-7): Photoresist patterning on back-side of membrane.

4.4.0 Exposure

The Research Devices Inc. Pattern Generator was used as a direct write exposure system to expose the coil pattern on the membrane. A mask file of the spiral coil was generated using a customized version of AutoCAD. The RDI system exposes regions drawn in the mask file. This means that in order to fabricate the coil on the membrane, metallization using lift-off would be needed.

Since the coil is to be fabricated inside the etched hole, the photoresist is spun on the back of the wafer. Conventional UV exposure would require the photoresist to be exposed with the UV light on the back of the wafer as shown in Fig. (4-8). The problem of exposing in this way is that it produces a sloping photoresist profile. Since it was determined that lift-off needs to be performed, this profile is undesirable.

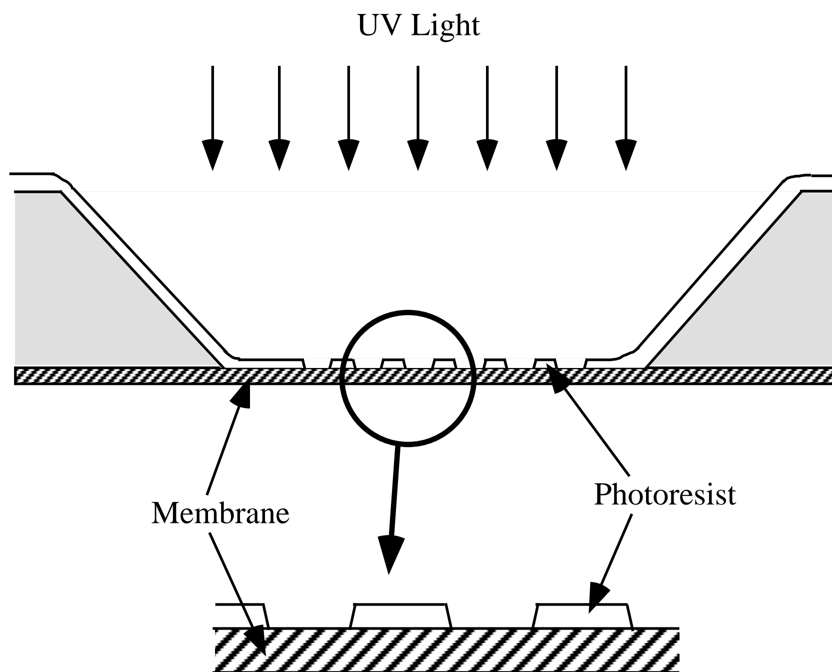


Fig. (4-8): The conventional exposure system.

Shown in Fig. (4-9) is the exposure method used to expose the coil shown in Fig. (4-7). As can be see from the figure (Fig. (4-9)) this produces an 'overhang' type of resist profile which is ideal for metal lift-off. Also for the 405 nm UV light used the imaginary part of silicon-dioxide and silicon-nitride is almost zero [5]. The real part is 1.47 for silicon-dioxide and 2.099 for silicon-nitride. This means that the membrane almost transparent to the UV light.

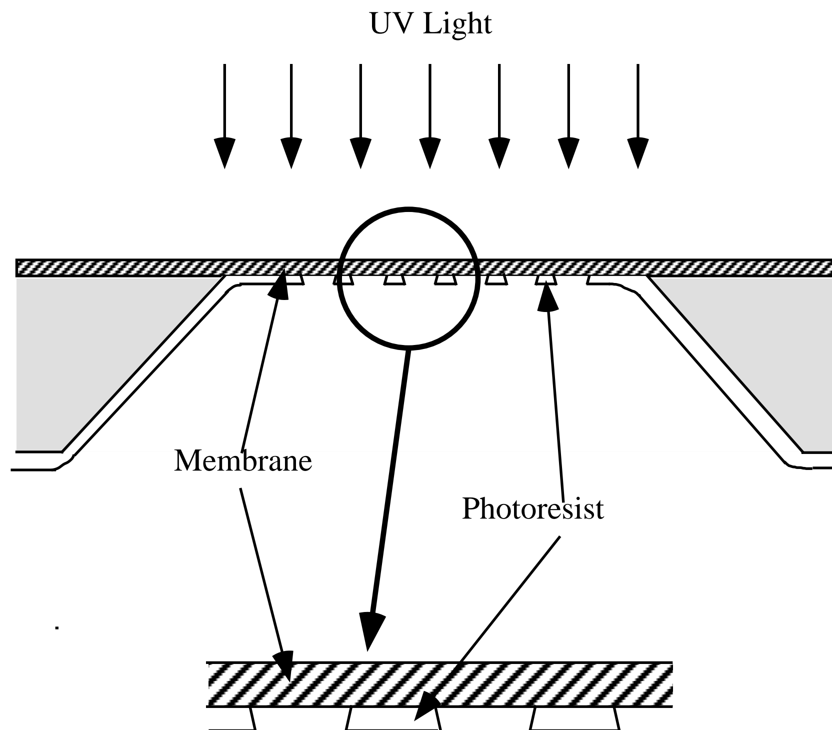


Fig. (4-9): Exposure through the membrane.

4.5.0 Patterning along the side walls

Etching a hole in a <100> wafer produces a pyramidal hole with the bounding <111>

planes at an angle of 54.74° to the horizontal. Also since the wafer is about 300 μm thick, this produces a depth of focus issue if conventional exposure techniques are used. In order to solve this problem the "autofocus" function of the RDI pattern generator can be used. By including "autofocus blocks" in the AutoCAD mask design, the RDI pattern generator can be programmed to perform an "autofocus" routine to keep the substrate in focus as it exposes the photoresist. Thus the mask level for the interconnects can include the "autofocus blocks" so that the RDI pattern generator keeps refocusing on the substrate as it moves along the side walls solving the depth of focus issue.

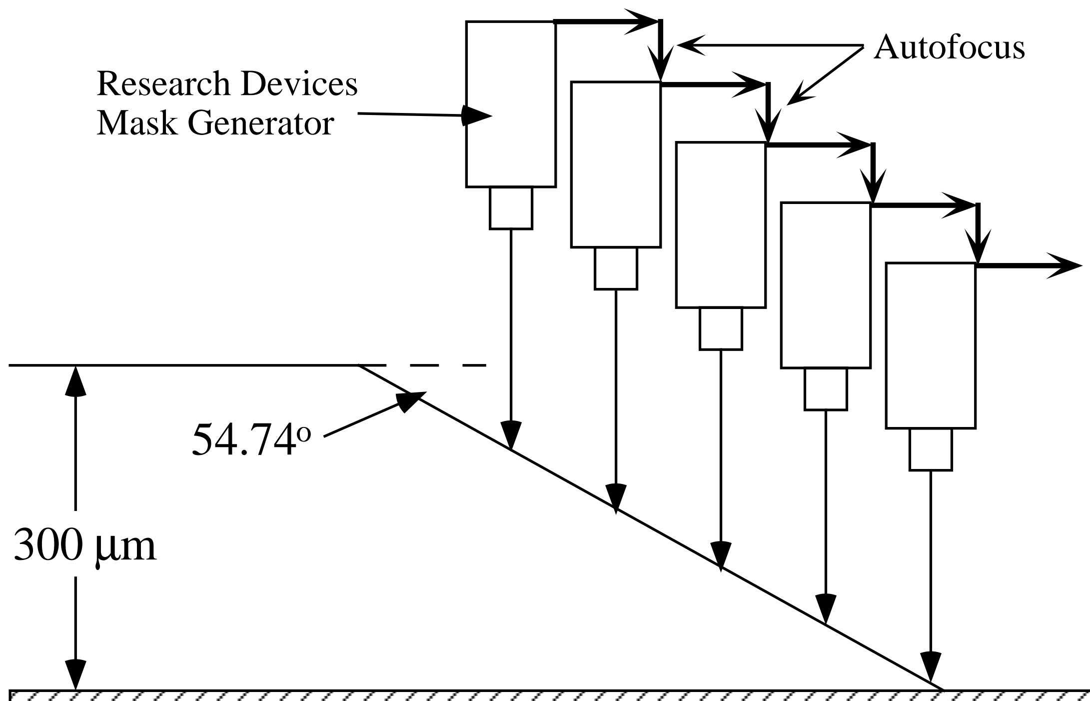


Fig. (4-10): Using the "autofocus" function of the RDI Pattern Generator to expose patterns along the side walls of the etched hole.

4.6.0 Summary

In this chapter various fabrication issues arising from fabricating the coil inside an etched hole have been discussed. The overhang issue was solved by making a square hole aligned to the crystal axes. The effect of the position of the hole with respect to the spin axis during the spinning of photoresist was also discussed. The four hole sample showed the best results and was used to fabricate the coil. The issue of patterning the side walls for the interconnects was also briefly discussed.

References

[1] L. Ristic, *Sensor Technology and Devices*, Norwood, MA: Artech House, INC., 1994.

[2] K. E. Petersen, *Silicon as a Mechanical Material*, Proceedings of the IEEE, vol. 70, pp. 39, 1982.

[3] J. J. W. Faust, and E. D. Palik, *Study of the Orientation Dependent Etching and Initial Anodization of Silicon in Aqueous KOH*, Journal of the Electrochemical Society: Solid-State Science and Technology, vol. 130, pp. 1413, 6 1983.

[4] A. Reisman, M. Berkenblit, S. A. Chan, F. B. Kaufman, and D. C. Green, *The Controlled Etching of Silicon in Catalyzed Ethylenediamine-Pyrocatechol-Water Solutions*, Journal of the Electrochemical Society: Solid State Science and Technology, vol. 126, pp. 1406, 8 1979.

[5] E. D. Palik, *Handbook of Optical Constants*, Florida: Academic Press, INC., 1985.