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Robert James Friar

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Analysis, Design, and Measurement of On-Wafer Transmission Line Test Structures

by

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Dissertation

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To K.K., for patience, understanding, and love.

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New dielectrics are being developed for integrated circuit applications, especially materials whose dielectric constant is less than that of silicon dioxide (i.e., so-called low-k dielectrics). The loss and relative dielectric constant of these materials needs to be characterized as a function frequency into the tens of GHz. It is desirable to characterize these materials in test structures with geometries that resemble integrated circuit interconnects.

This dissertation examines the effect of S-parameter measurement errors on the characterization of microstrip test structures. First, a perturbation technique is used to analyze the effect of S-parameter errors on the extraction of transmission line parameters; both magnitude and phase errors are considered. Next, derivative-based error propagation is used to design test structures that are minimally affected by the S-parameter errors. Finally, data from on-wafer microstrip test structures are compared to results from both the perturbation and derivative techniques.

The results of this study indicate that geometry significantly affects the transmission line parameter extraction error. The method presented designs test structures that minimize the extraction error for a set of geometrical and material constraints.

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