Special Processes

- wide variety of processes used in mems fabrication that are not “standard” IC fabrication
  - anisotropic crystallographic etches
    - KOH etch uses a mobile ionic contaminant!
- many processes used in other applications can be adapted
  - laser drilling, laser sintering, injection molding, solid free-form fabrication, electric discharge machining (EDM), etc
    - potential disadvantage for “volume” production: many of these are not “parallel” or “batch” processes

Electrodeposition/electroplating

- classical industrial process used to produce thin coatings
  - almost always metal
  - deposition is from the liquid phase, driven by an electrochemical reaction
    - solution generally contains an ion of the metal (a “salt) that is easily reduced
    - application of a negative bias to object to be plated (i.e., the object is the cathode) supplies the electrons necessary for reduction, resulting in deposition on the cathode
      - local rate of deposition proportional to local current density
    - J-V characteristic exhibits a saturation behavior
      - above a certain applied voltage the current density saturates
      - applied potential above this max tends to drive things like electrolysis of water, rather than reduction of the metal salt
        - porous, poor quality deposition tends to result
        - “black” metal at high current density

Electroplating examples

- copper
  - usually copper sulfate in sulfuric acid
    - Cu^{2+}(solution) + $2e^-$ ➔ Cu(solid)
  - few mAmp / cm^2
- gold
  - usually gold cyanide solution
    - $Au(CN)_2^-$ ⇔ AuCN + CN^-
    - AuCN + e^- ➔ Au(solid) + CN^-
  - few tens-hundred mA / cm^2
- nickel
  - nickel sulfate, boric acid
- masking
  - photoresist or other non-conducting layer can be used
  - for small, complex shapes must be careful about
    - depletion of reactants
    - non-uniformity in current density
    - crystallographic orientation dependent growth rates

Liga

- "Lithographie, Galvanoformung, Abformung"
  - Ehrfeld et al, mid-80's; Guckel at Wisconsin
  - "lithography, electroplating, and molding"
    - really is just masked electroplating, but with high aspect ratio mask layers
    - biggest challenge is the high aspect ratio lithography
      - use X-ray proximity lithography
      - recall

$$l_{\min} \approx \frac{3}{2}\sqrt{gap \cdot \lambda}$$

      - gap ~ thickness of resist ~ 100μm
      - x-ray wavelength ~ 0.01μm
      - ⇨ l_{min} ~ 1μm ⇨ 100:1 aspect ratio feature

Anodic oxidation

- anodization
  - sample connected to positive terminal of dc supply
    - sample is the anode
  - immersed in an electrolyte
    - usually aqueous, but regardless oxidizing species is almost always $(OH)^-$
- basic mechanism
  - injection of holes into Si to form Si^{2+} ("anodic" reaction)
  - attachment of OH^- to the Si^{2+} to form $Si(OH)_2$ (oxidation step)
  - reaction of the "hydrated silica" to form oxide and hydrogen
- overall reaction for silicon oxidation
  - $Si + 2h^+ + 2H_2O \rightarrow SiO_2 + 2H^+ + H_2$
  - holes supplied by bias supply
  - H^+ migrates to cathode, ultimately produces H_2 at cathode

Anodic oxidation kinetics

- constant voltage bias
  - thickness builds exponentially in time to a final asymptotic value
    - $x = x_\infty (1 - e^{-t/\tau})$
    - for silicon $x_\infty \sim 3Å / V$
      - i.e., for V =1000V the final thickness would be about 0.3μm
- constant current bias
  - thickness is linearly increasing in time
  - voltage also increasing in time
    - still have $x_\infty \sim 3Å / V$

Bonding processes

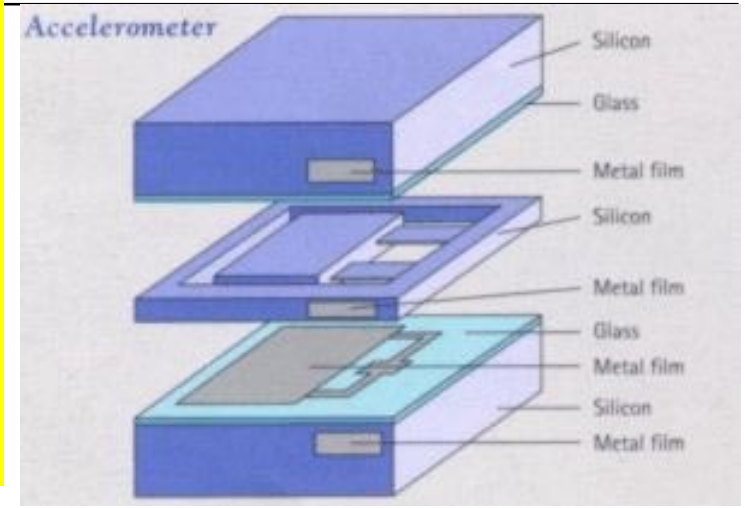
- general requirements
  - TCE match for dissimilar materials
- adhesives
  - “bond line” thickness, long term hermeticity, out-gassing
  - single component, multi-component, aerobic, anaerobic, UV-curable
- metal-glass seals
  - with appropriate glass and metal choice extremely high quality bonds can be formed, but usually requires T ~ 1000°C
- silicon - silicon fusion bonding
  - usually fairly high temperature: ~1000C
  - surfaces should be hydrophilic, interaction via “oxide” at interface

Anodic bonding

- example: silicon to Pyrex 7740
  - ~ 400°C, ~ 1kV applied voltage
  - reasonable TCE match
  - glass is ionic conductive at moderate temperatures
    - current does flow, but electrode contacts are non-injecting
      - at constant voltage, initial current is high (~mA/cm^2), decays with time
      - leads to depletion layer formation at silicon – glass interface
  - use electric field helps provide force to pull mating surfaces together
  - actual bond via oxidation of silicon surface intermixing with glass surface

wafer bonding

Technical Data
Wafer/Substrate Parameter: Up to 150mm
Max. wafer stack thickness 4 mm
Wafer/Substrate Configuration: Double stack: Silicon/Glass, Silicon/Silicon
Triple stack: Any combination of Silicon and Glass
Pressure Chamber: Over pressure: 2 bar (29 psi)
Vacuum: 5 E-3 mbar – standard
1 E-5 mbar high vacuum optional
Heater: 550 °C max.
Voltage: 0 - 1200V / 50 mA
optional up to 2000V / 50mA and 250V / 3A
Contact Pressure: Up to 3.4 kN (765 lbf)
optional up to 7 kN max (1570 lbf)



http://www.evgroup.com/products/waferbonding.htm

Drying

- problem: for two closely spaced layers during rinsing and subsequent drying capillary forces may cause collapse and sticking (stiction)
- methods
  - critical point drying
    - at appropriate temperature, pressure liquid and gas are “same”: supercritical region of phase diagram
    - example: CO_2: T > 31.1°C, P > 72.8 atm
  - phase change drying
    - freeze, then sublime
  - low surface tension rinsing
    - alcohol
  - surface treatments