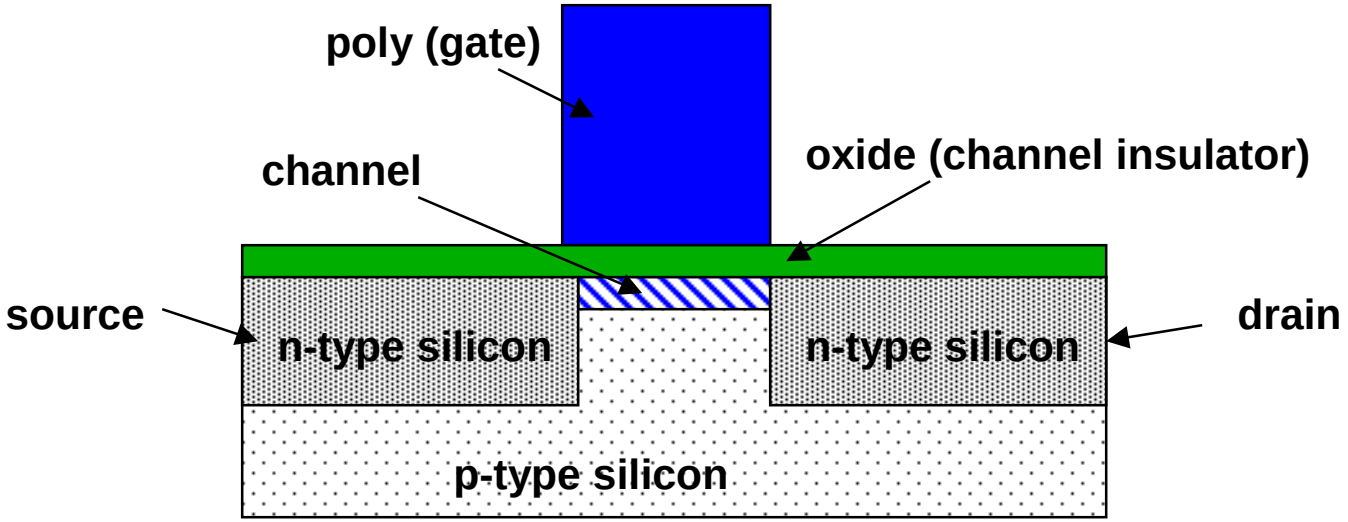
“Classical” IC fabrication overview: How to make a MOSFET

- What do you need?
  - a good semiconductor (SILICON)
  - a p-n junction (boron-doped Si - phosphorus-doped Si)
  - a good insulator (SILICON DIOXIDE)
  - a good conductor (poly-silicon and aluminum, copper)

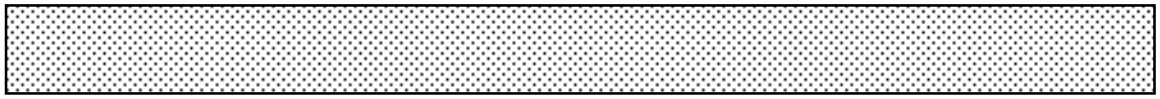


Silicon Device Processing

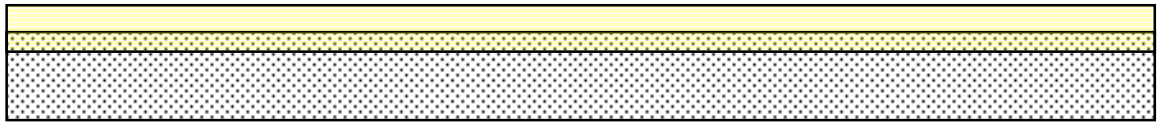
- The construction of a silicon integrated circuit uses three basic processes:
  - Oxidation:
    - by heating silicon to about 1000°C in oxygen the surface of the silicon becomes silicon dioxide (glass), a very good insulator.
  - Photolithography:
    - is a way of producing a pattern of bare areas and covered areas on a substrate. This serves as a mask for etching of the silicon dioxide.
  - Doping:
    - processes used to introduce controlled amounts of impurities into the bare areas on the silicon (as little as one impurity atom per million silicon atoms). This allows the formation of p-n diodes in the substrate.
- When all these steps are combined, along with metal wires for connections between devices, an integrated circuit can be made.

How to make a MOSFET

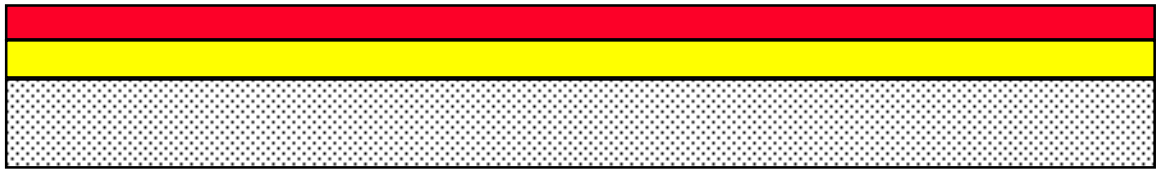
start: bare silicon wafer



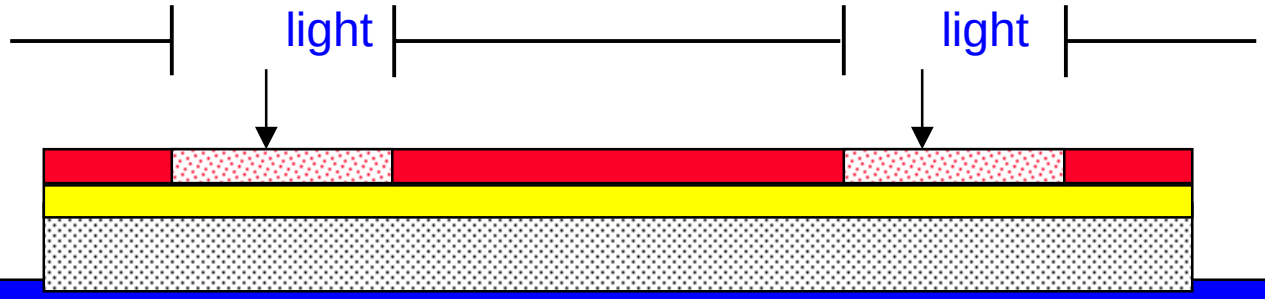
oxidize



apply *photoresist* (pr)

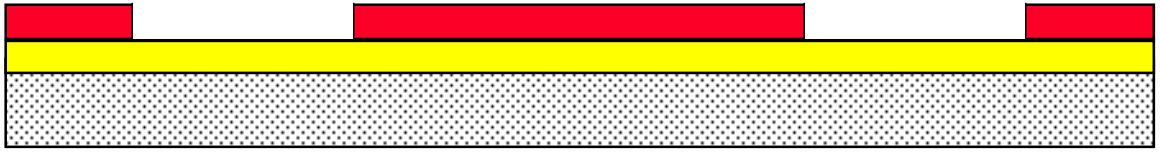


expose mask 1

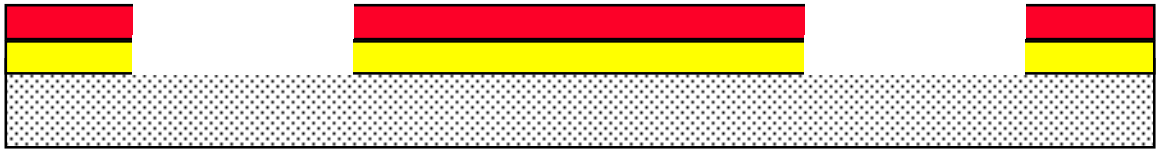


How to make a MOSFET

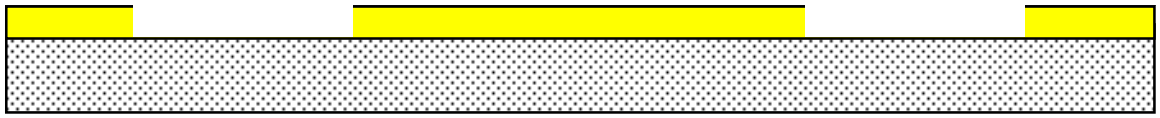
develop pr



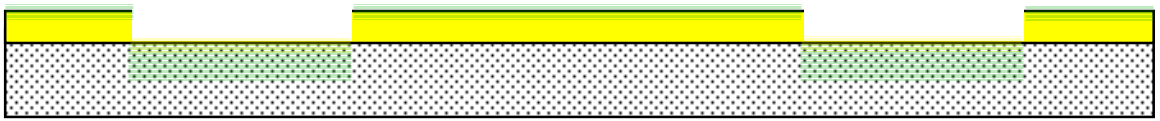
etch oxide



strip pr

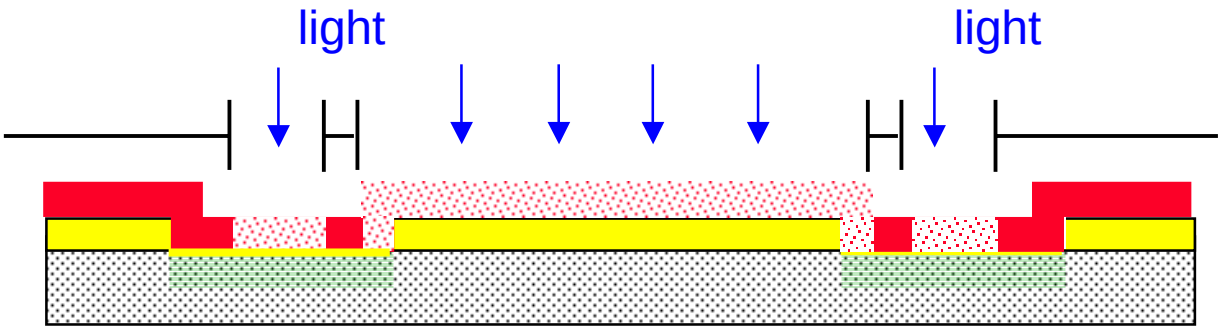


introduce source drain dopants



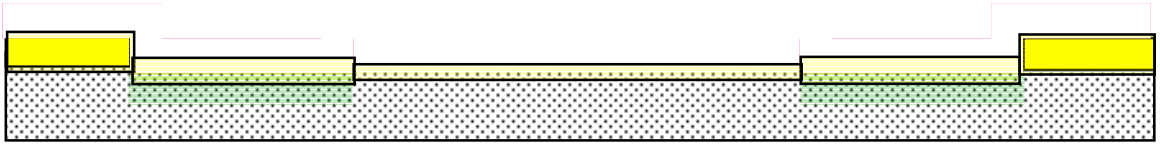
How to make a MOSFET

coat pr, align mask 2, expose mask 2



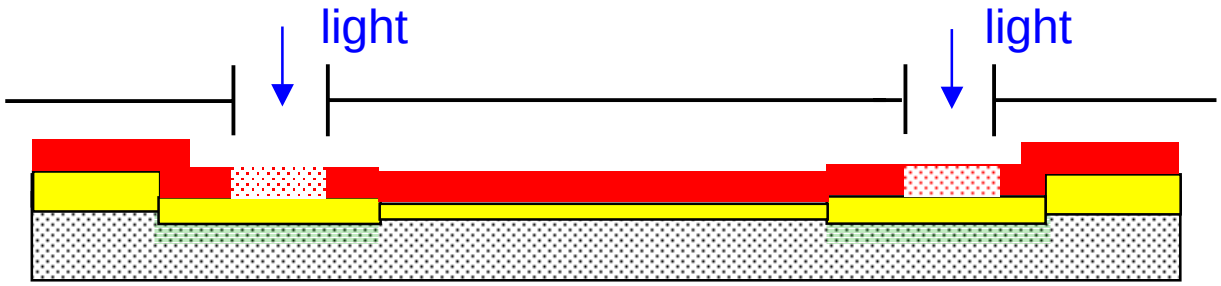
develop pr, etch oxide

strip pr, re-oxidize to form gate insulator

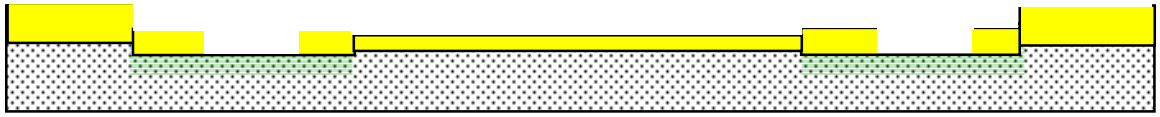


How to make a MOSFET

coat pr, align mask 3, expose mask 3

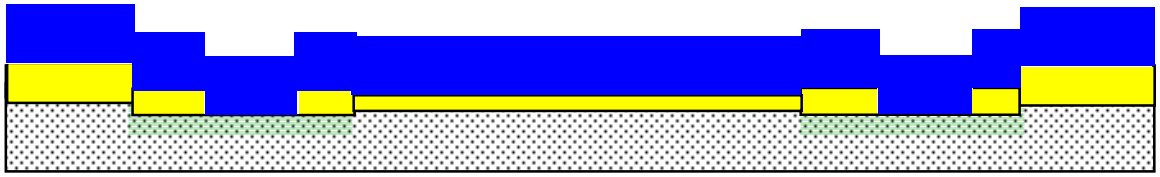


develop pr, etch oxide, strip pr

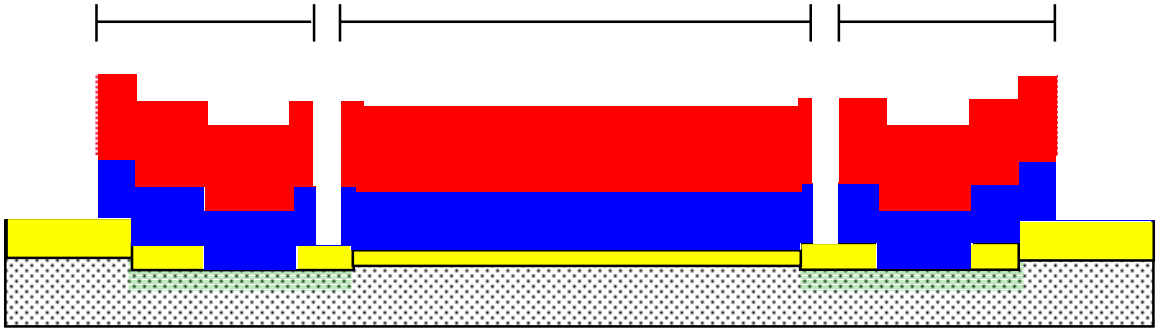


How to make a MOSFET

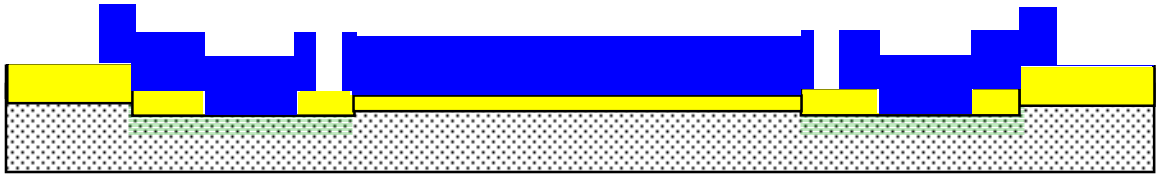
metallize,



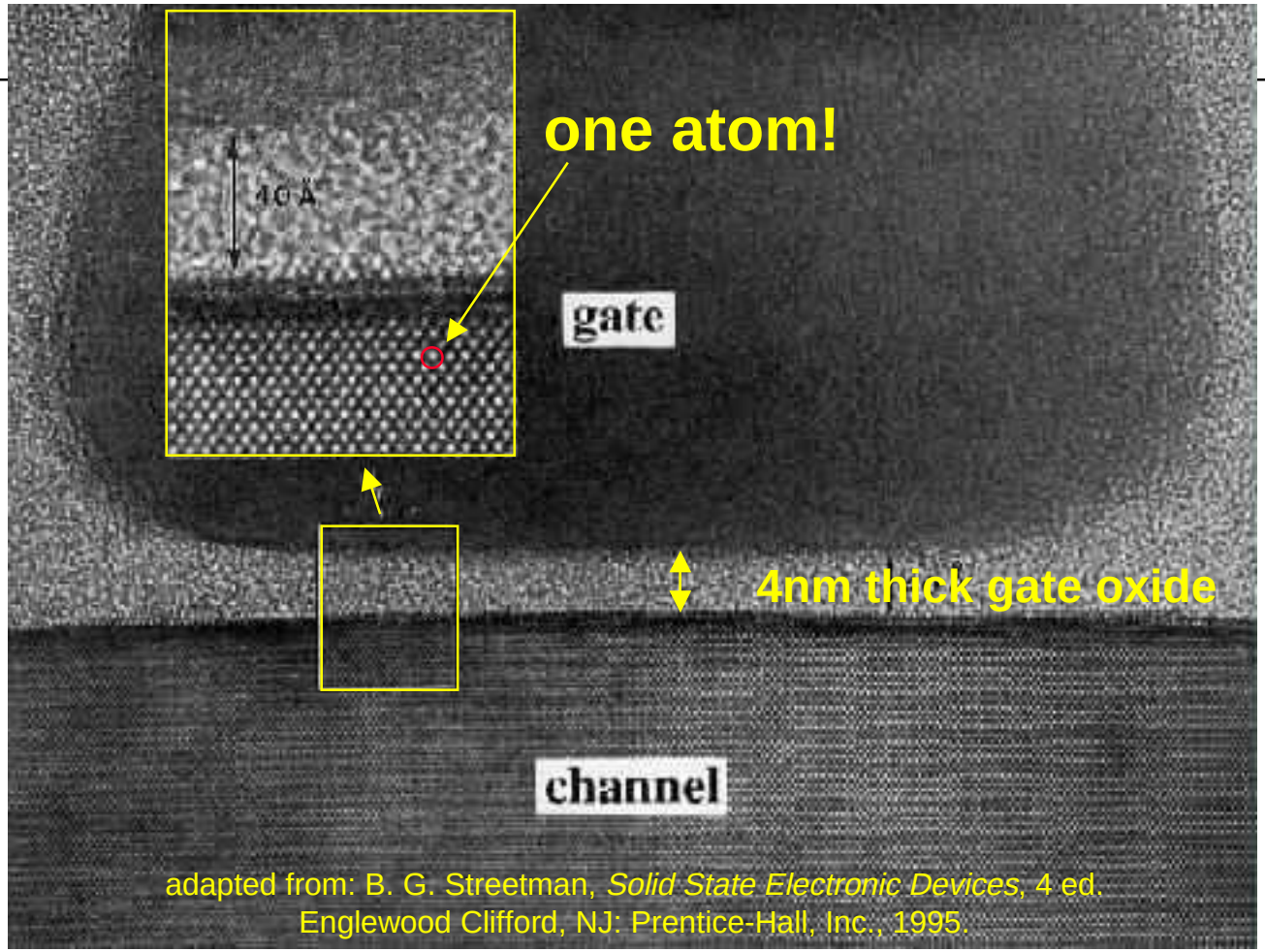
coat pr, align mask 4, expose, develop pr, etch metal



strip pr: FINISHED!



MOSFET cross section



adapted from: B. G. Streetman, *Solid State Electronic Devices*, 4 ed. Englewood Clifford, NJ: Prentice-Hall, Inc., 1995.

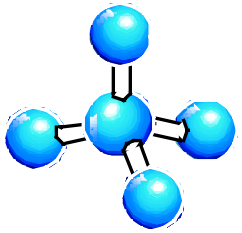
- **modern integrated circuits contain millions of individual MOSFETS**

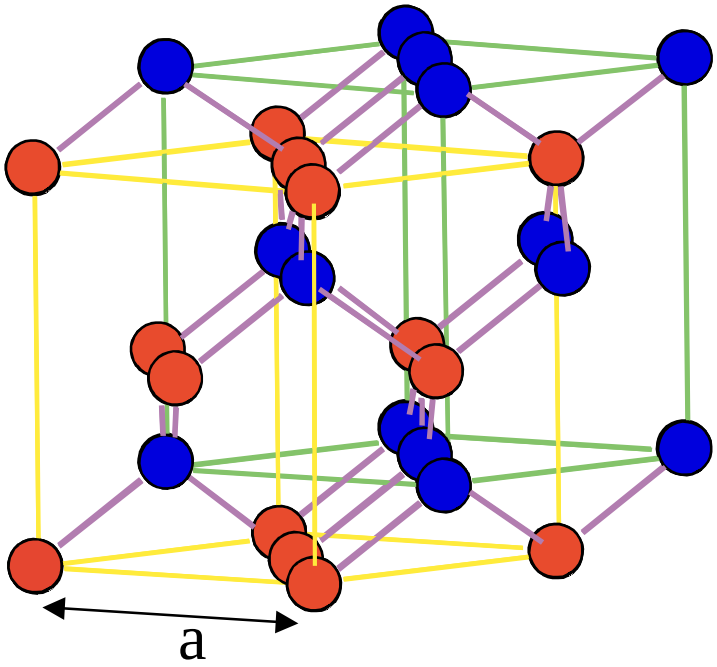
Silicon as a mechanical material for MEMS fabrication

- **classic reference in the field:**
  - **K.E. Petersen "Silicon as a Mechanical Material", *Proceedings of the IEEE*, Vol. 70, No.5, May 1982.**
    - **http://robotics.eecs.berkeley.edu/~tahhan/MEMS/petersen/mems_petersen.htm**
  - **tenants:**
    - **silicon is abundant, inexpensive, and can be produced in extremely high purity and perfection;**
    - **silicon processing based on very thin deposited films which are highly amenable to miniaturization;**
    - **definition and reproduction of the devices, shapes, and patterns, are performed using photographic techniques that have already proved of being capable of high precision;**
    - **silicon microelectronic (and therefore also mems) devices are batch-fabricated.**

Silicon crystal structure

- valence 4 structure
  - each atom bonds to four neighbors in a tetragonal configuration
- crystal lattice is face centered cubic (FCC), with two atom basis [at (0,0,0) and (1/4, 1/4, 1/4)]: Zincblende
  - two "interpenetrating" FCC lattices
  - lattice constant "a": cube side length
    - silicon (rm temp): 5.43 Å
    - nearest neighbor distance $d_n = \frac{\sqrt{3}}{4} a$
  - atomic density:
    - 4 atoms inside cube
    - 6 atoms "half" inside at face centers
    - 8 atoms 1/8 inside at corners
    - total of 8 atoms per cube: atomic density $8 / a^3$





$\rho_{Si} = 5 \times 10^{22}$ atoms/cm^3

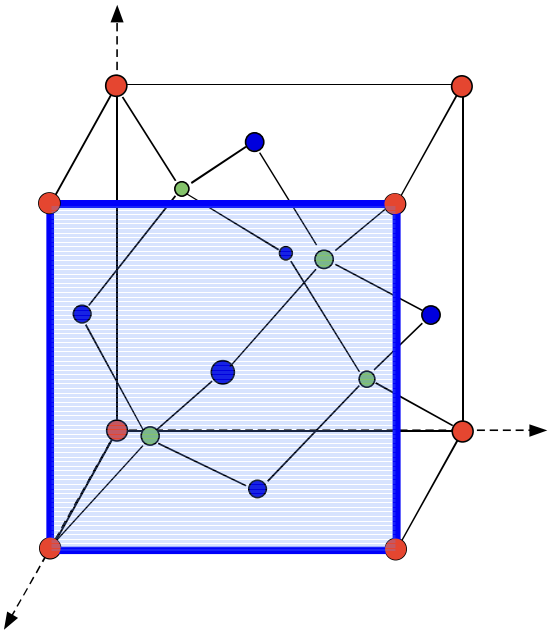
Miller Indices in Crystals

- **For a plane with:**
  - **x-axis intercept x_o**
  - **y-axis intercept y_o**
  - **z-axis intercept z_o**
  - **the Miller indices (hkl) for this plane are given by finding the inverses of x_o, y_o, & z_o and reducing them to the smallest set of integers h: k: l having the same ratio $(x_o)^{-1}$: $(y_o)^{-1}$: $(z_o)^{-1}$.**

- **Conventions:**
  - **(hkl): single plane or set of all parallel planes.**
  - **($\bar{h}$ kl): for a plane that intercepts the x axis on the negative side of the origin.**
  - **{hkl}: for all planes of equivalent symmetry, such as {100} for (100), (010), (001), ($\bar{1}$00), (0$\bar{1}$0), and (00$\bar{1}$) in cubic symmetry.**
  - **[hkl]: for the direction perpendicular to the (hkl) plane.**
  - **<hkl>: for a full set of equivalent directions.**

Low Index Directions In Silicon (Cubic, Diamond Structure)

- **(100)**



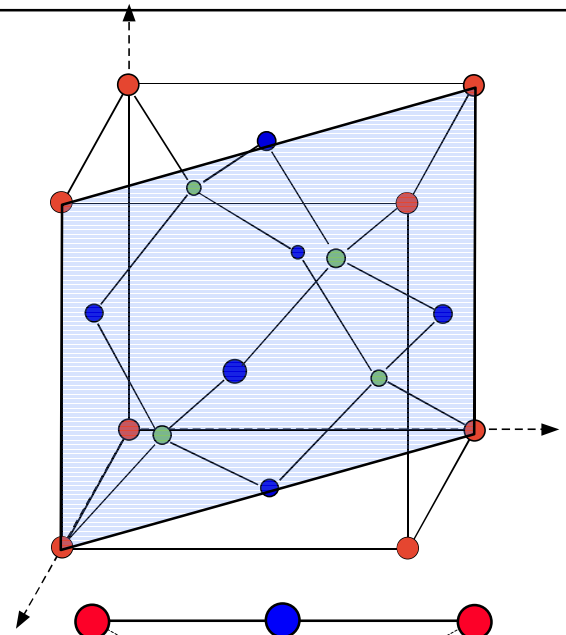
surface atomic density

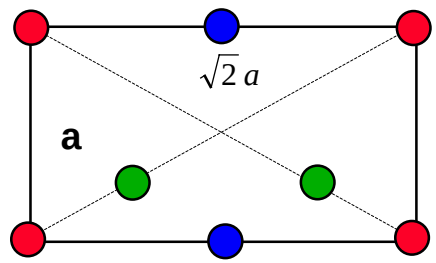
$$\rho_{100}^{surface} = \frac{\left(1atom + 4 \cdot \left[\tfrac{1}{4} atom\right]\right)}{a^2}$$

silicon:

ρ_{100} **= 6.8 x 10^{14} atoms / cm²**

- **(110)**

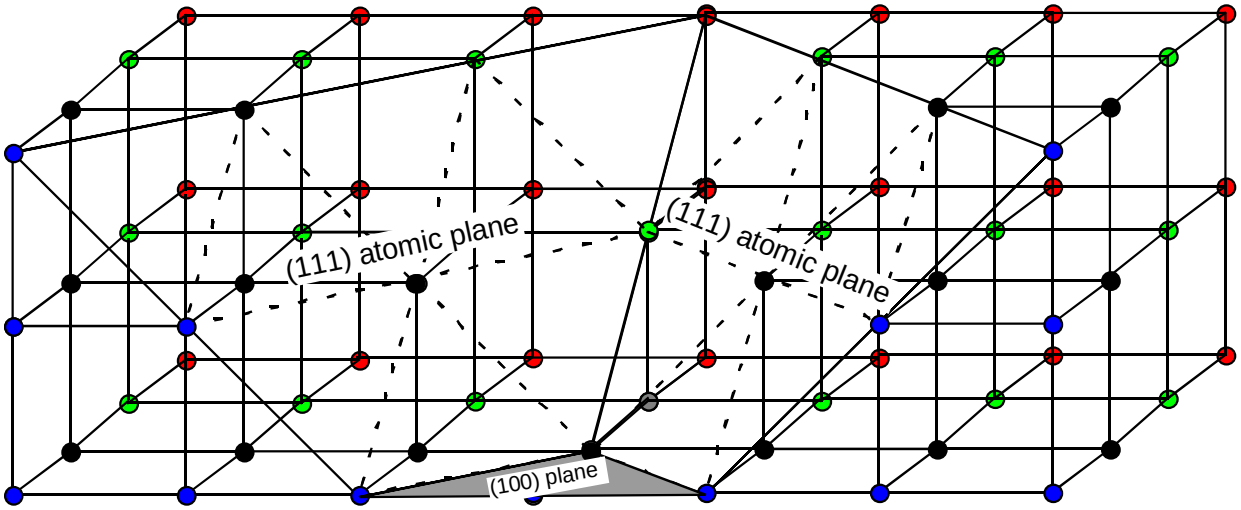


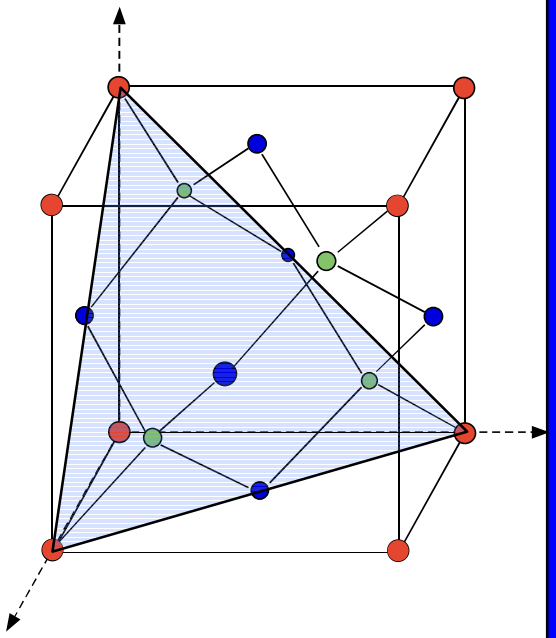


$$\rho_{110}^{surface} = \frac{\left(2\,\text{atoms} + 4 \cdot \left[\tfrac{1}{4}\,\text{atom}\right] + 2 \cdot \left[\tfrac{1}{2}\,\text{atom}\right]\right)}{\sqrt{2}\,\text{a} \cdot \text{a}}$$

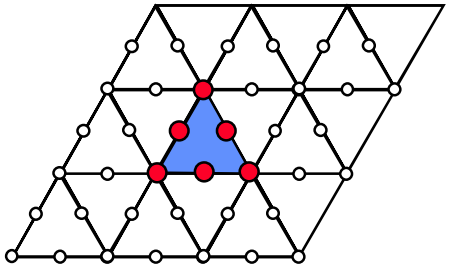
(111) planes

- **(111) planes etch the slowest, tend to be cleavage planes**





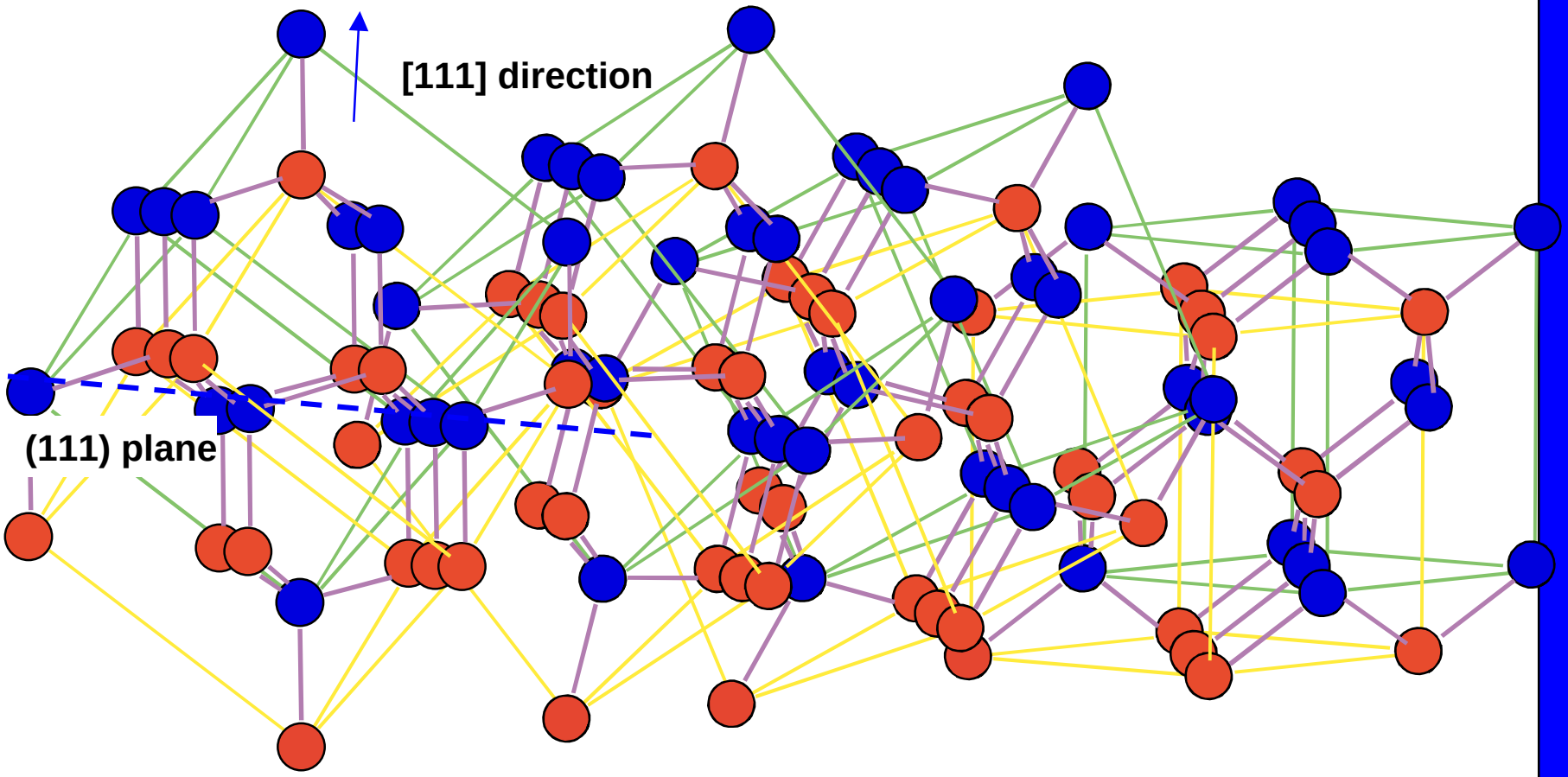
$$\rho_{111}^{\text{surface}} = \frac{\left(3 \cdot \left[\tfrac{1}{2}\ \text{atom}\right] + 3 \cdot \left[\tfrac{1}{6}\ \text{atom}\right]\right)}{\sqrt{3}/2 \cdot a^2}$$



- **silicon:**
  7.8×10^{14} atoms / cm^2
- **surface atomic density somewhat higher than (100)**

(111) orientation in silicon

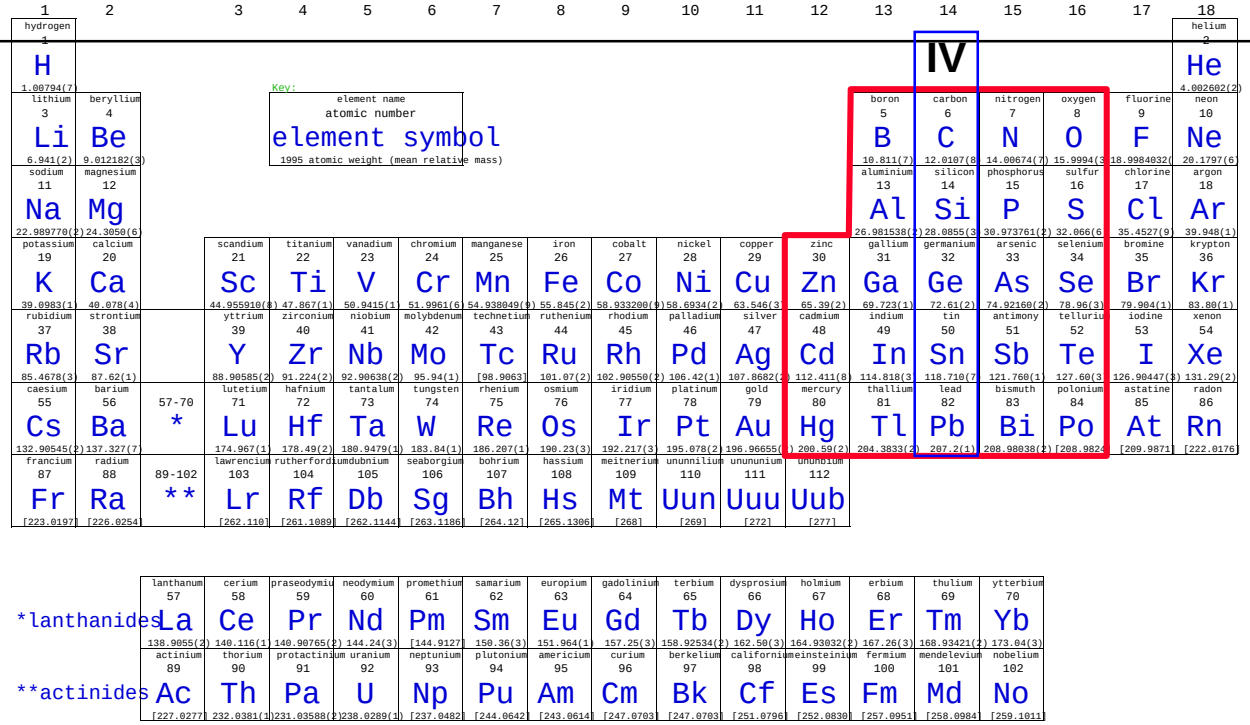
- [111] is the “natural” orientation for zincblende crystals



Dopants and impurities in semiconductors

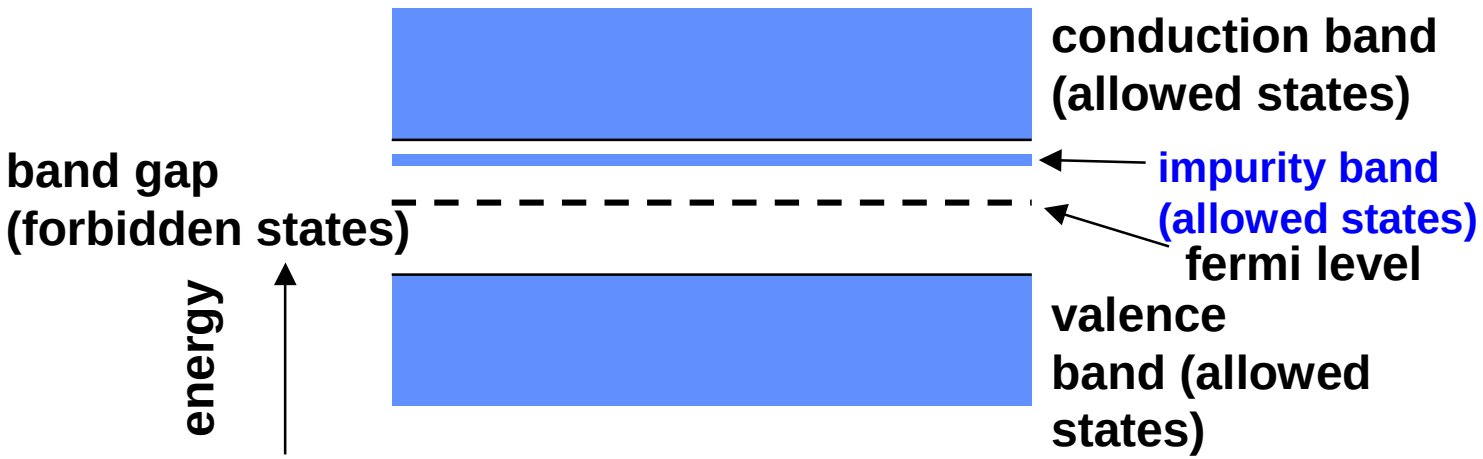
WebElements: the periodic table on the world-wide web

http://www.shef.ac.uk/chemistry/web-elements/



- **For column IV elements (e.g., silicon)**
  - **valence III: one electron “short”, acceptor**
    - **boron, aluminum, gallium**
  - **valence V: one “extra” electron, donor**
    - **nitrogen, phosphorus, arsenic, antimony**

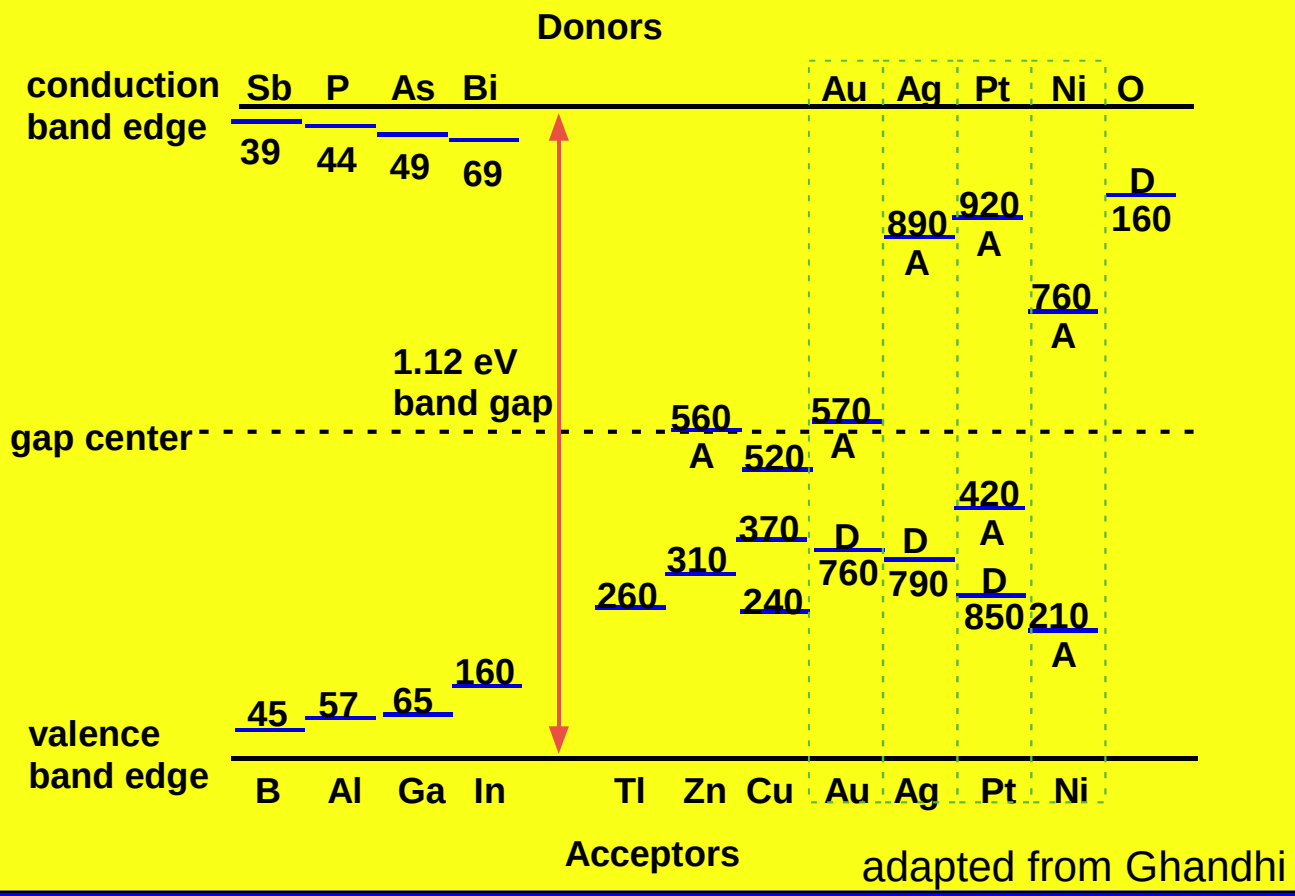
Band diagrams for semiconductors



- Fermi level indicates how states are actually occupied
  - a flat fermi level indicates that no external voltages are applied
  - most above the Fermi level are empty of electrons
  - most below are full of electrons
    - donor levels are empty when "active"
    - acceptor levels are occupied when "active"

Impurities in silicon

- impurity levels in meV from band edge
  - A: acceptor-like behavior
  - D: donor-like behavior



adapted from Ghandhi

Impurities in Silicon

- **Oxygen: (column VI)**
  - **common unintentional impurity from silica crucibles**
    - **10^{16} - 10^{18} cm^{-3}**
    - **usually clumps with silicon into large (~1μm) SiO_2 complexes; sensitive to processing history**
- **Carbon: (column IV)**
    - **high solid solubility ($4x10^{18}$)**
    - **mainly substitutional, electrically inactive**
- **Gold:**
    - **deep donor or acceptor**
    - **rapid diffuser**
    - **minority carrier lifetime "killer"**

Solid solubility limits in Si

- solid solubility: maximum equilibrium concentration of impurity (solute) in host material (solvent)
  - temperature dependent
  - generally lower at lower temp
  - @ 1000˚C

element $N_{solid\ sol}$ (cm^{-3})				
		B 1.5×10^{20}	C	N
		Al 2×10^{19}	Si	P 10^{21}
Cu	Zn	Ga 3×10^{19}	Ge	As 2×10^{21}
Ag	Cd	In	Sn	Sb 4×10^{19}
Au 10^{16}	Hg	Tl	Pb	Bi

Defects in crystals

- point defects
  - “zero” dimensional
  - most common, lowest energy of formation
- dislocations or line defects
  - one dimensional
  - collection of continuous point defects
- area (planar) defects
  - two dimensional
  - gross change in crystal “orientation” across a surface

Point Defects in Crystals

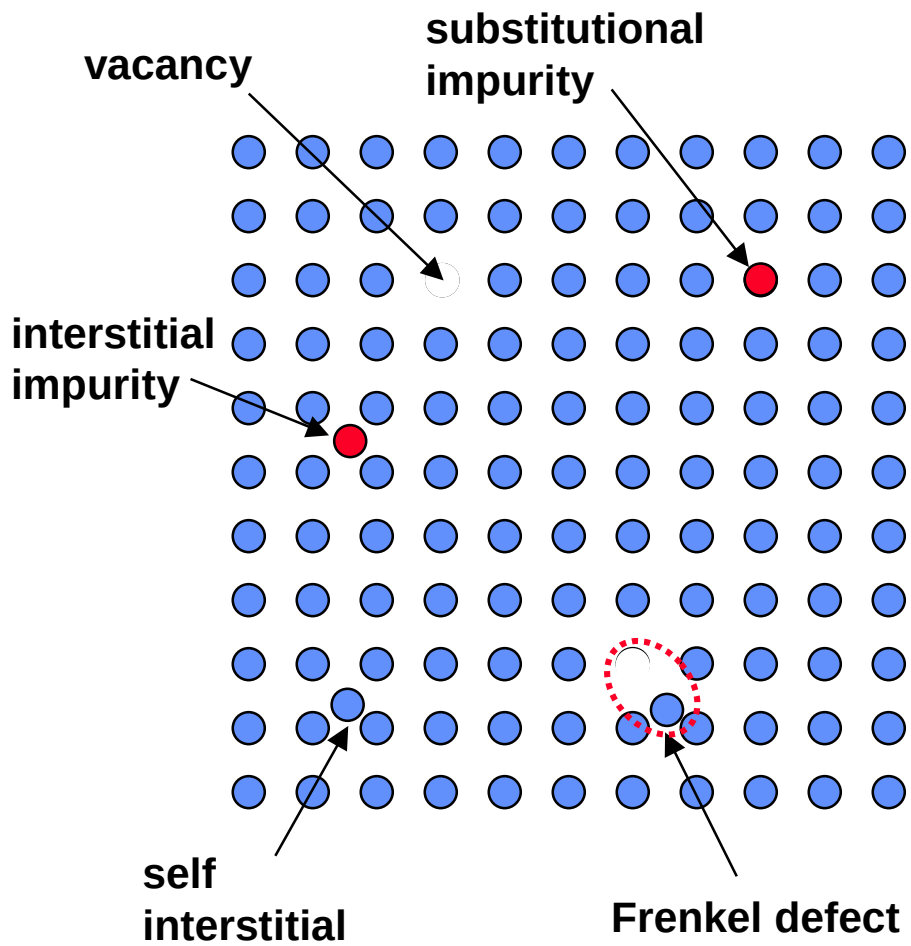
- vacancy , interstitial , substitutional
  - isolated vacancy: Schottky defect

    $$n \cong N_{atomic}\, e^{-E/kT}$$

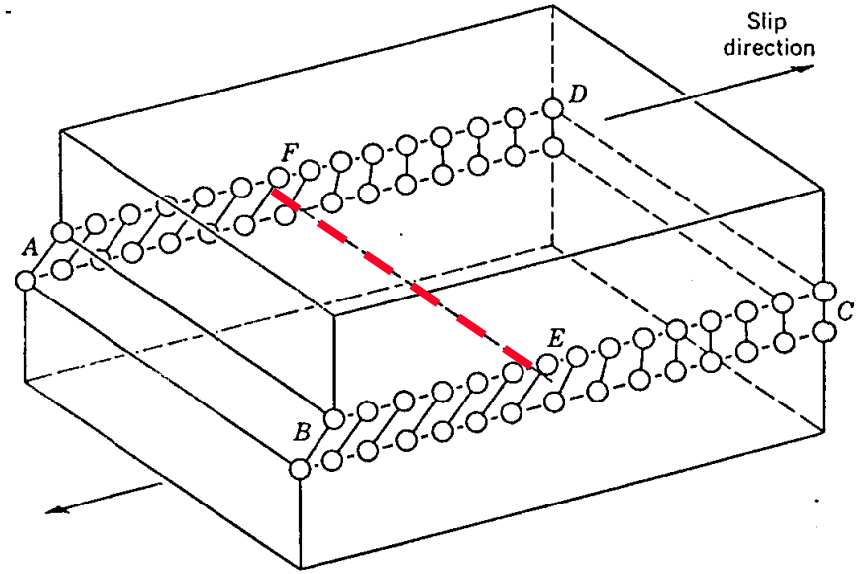
    - $E_{formation}$ ~ 2 eV
      - T = 300K: n ~ 0
      - T = 1300K: n ~ 10^{13}
  - vacancy-interstitial pair: Frenkel defect

    $$n \cong N_{atomic}\, e^{-E/2kT}$$

    - $E_{formation}$ ~ 1 eV
      - T = 300K: n ~ 10^{13}
      - T = 1300K: n ~ 10^{20}

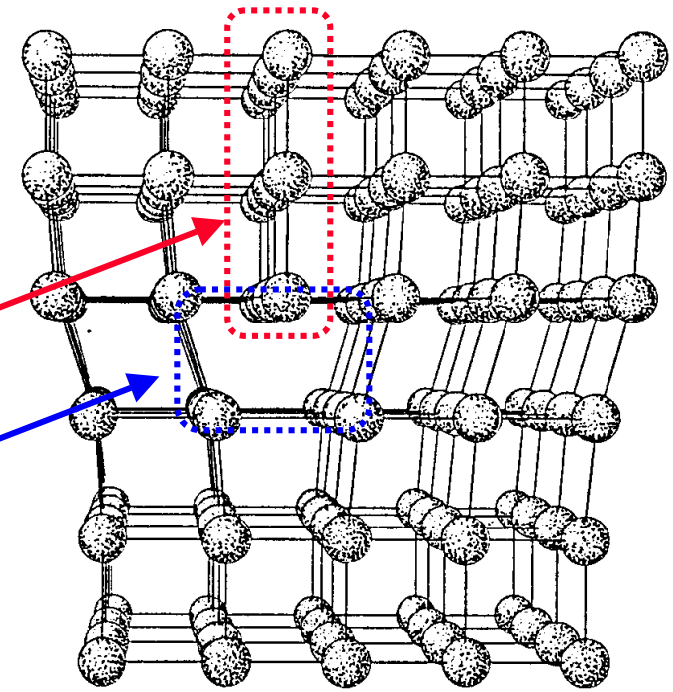


Edge Dislocations



$\overline{EF}$ is dislocation line

- one dimensional defect
  - formation energy is high, concentration usually low

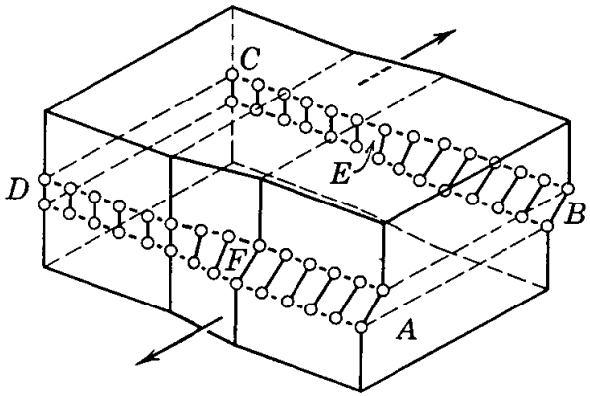


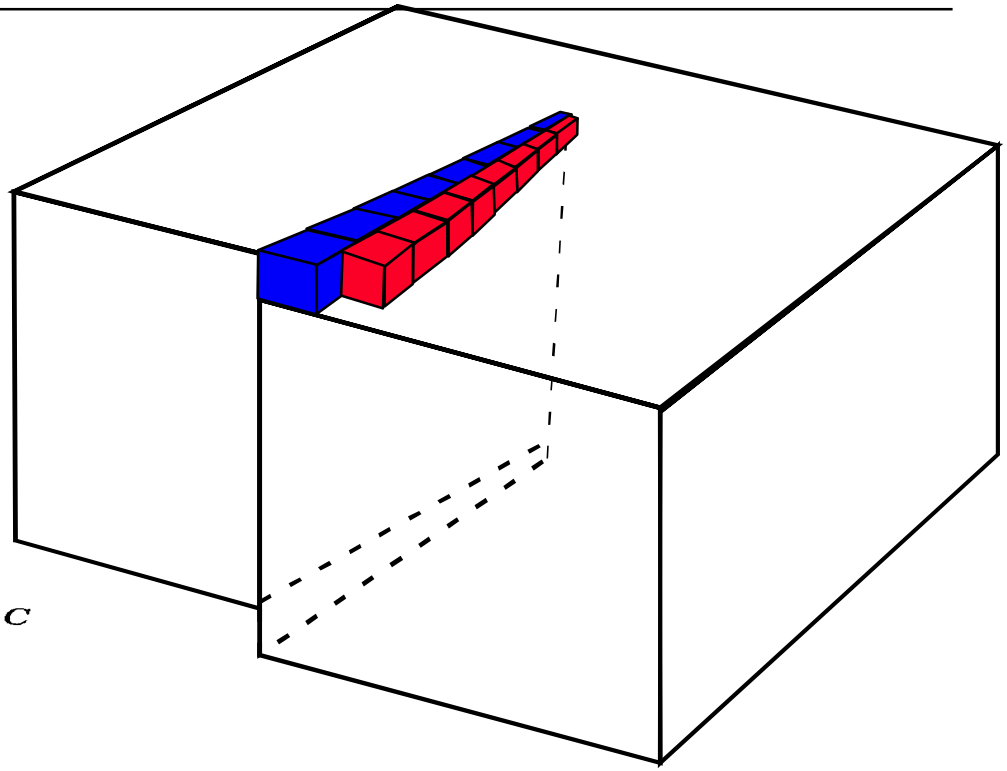
"extra" plane of atoms

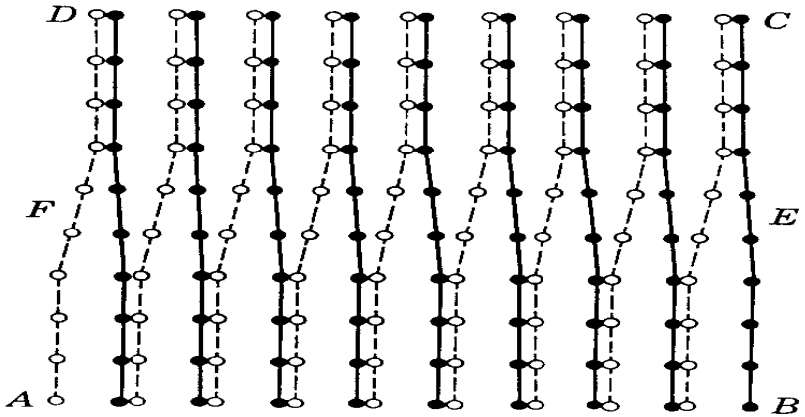
dislocation

from Kittel, p. 591

Screw Dislocation (1-d defect)







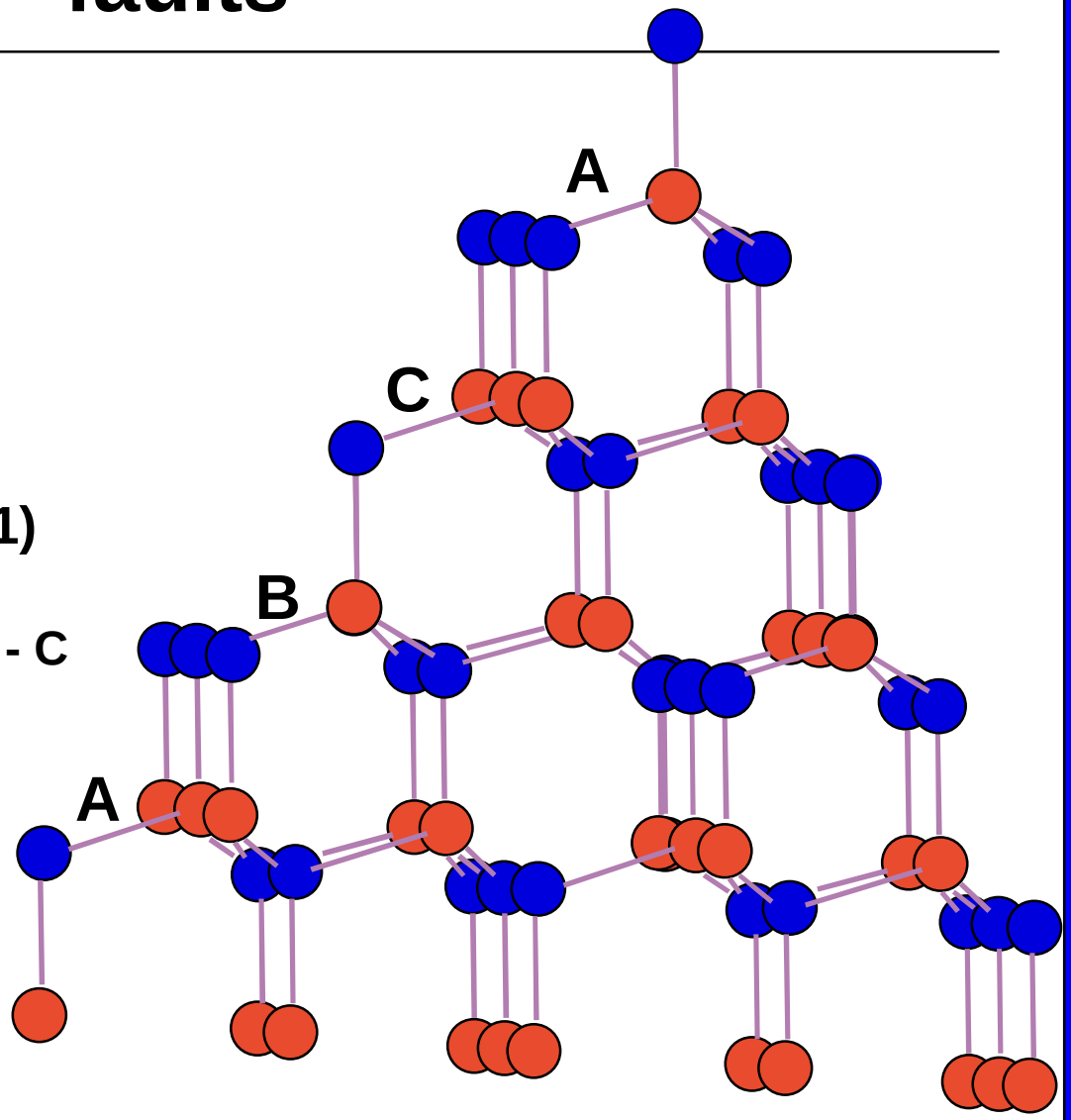
- **screw dislocations are most commonly formed during crystal growth**

Stacking arrangement and stacking faults

- layer ordering:

  A B C A B C

- planar (2-d) defect
  - stacking fault: missing or extra (111) plane
    - A - B - C - C - A - B - C
    - A - B - A - B - C



Bulk crystal growth

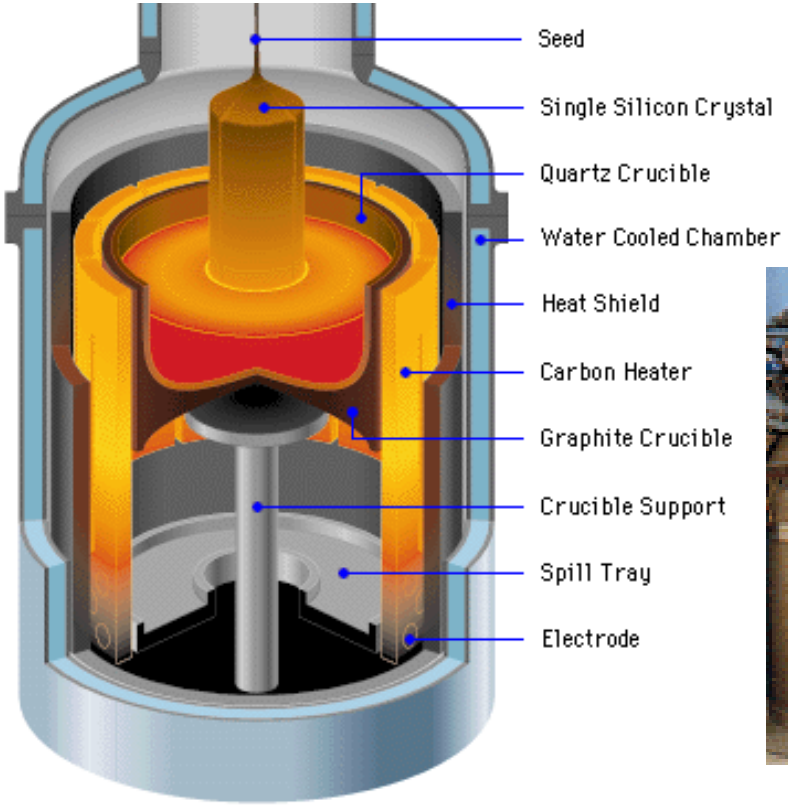
- melting points
  - silicon: 1420˚ C
  - quartz: 1732˚ C
- starting material: metallurgical-grade silicon
  - by mixing with carbon, SiO_2 reduced in arc furnace
    - T > 1780˚C:
      $SiC + SiO_2 \rightarrow Si + SiO + CO$
  - common impurities
    - Al: 1600 ppm (1 ppm = 5×10^{16} cm^{-3})
    - B: 40 ppm
    - Fe: 2000 ppm
    - P: 30 ppm
  - used mostly as an additive in steel

Preparation of electronic-grade silicon

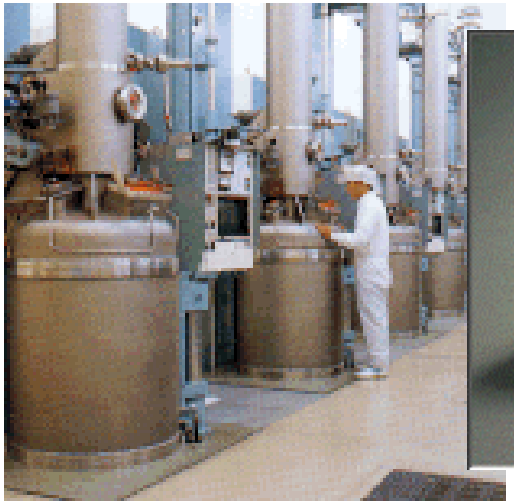
- gas phase purification used to produce high purity silicon
  - ~ 600˚C
  - crud + Si + HCl $\rightarrow$
    - $SiCl_4$ (silicon tetrachloride)
    - $SiCl_3H$ (trichlorosilane)
    - $SiCl_2H_2$ (dichlorosilane)
    - chlorides of impurities
  - trichlorosilane (liquid at rm temp), further purification via fractional distillation
- now reverse reaction
  - $2SiHCl_3 + 2H_2$ (heat) $\rightarrow 2Si + 6HCl$
  - after purification get
    - Al: below detection
    - B: < 1 ppb (1 ppb = 5×10^{13} cm^{-3})
    - Fe: 4 ppm
    - P: < 2 ppb
    - Sb: 1 ppb
    - Au: 0.1 ppb

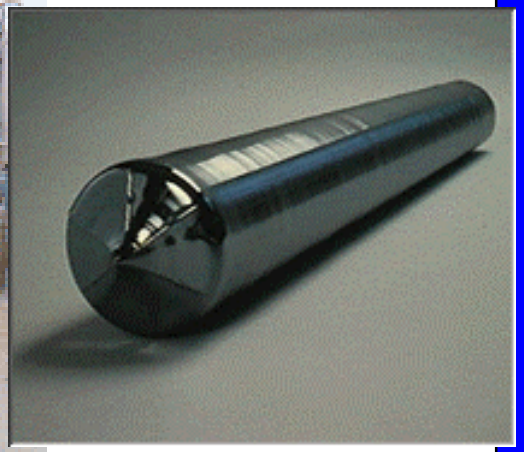
Czochralski crystal growth

- silicon expands upon freezing (just like water)
  - if solidify in a container will induce large stress
- CZ growth is “container-less”



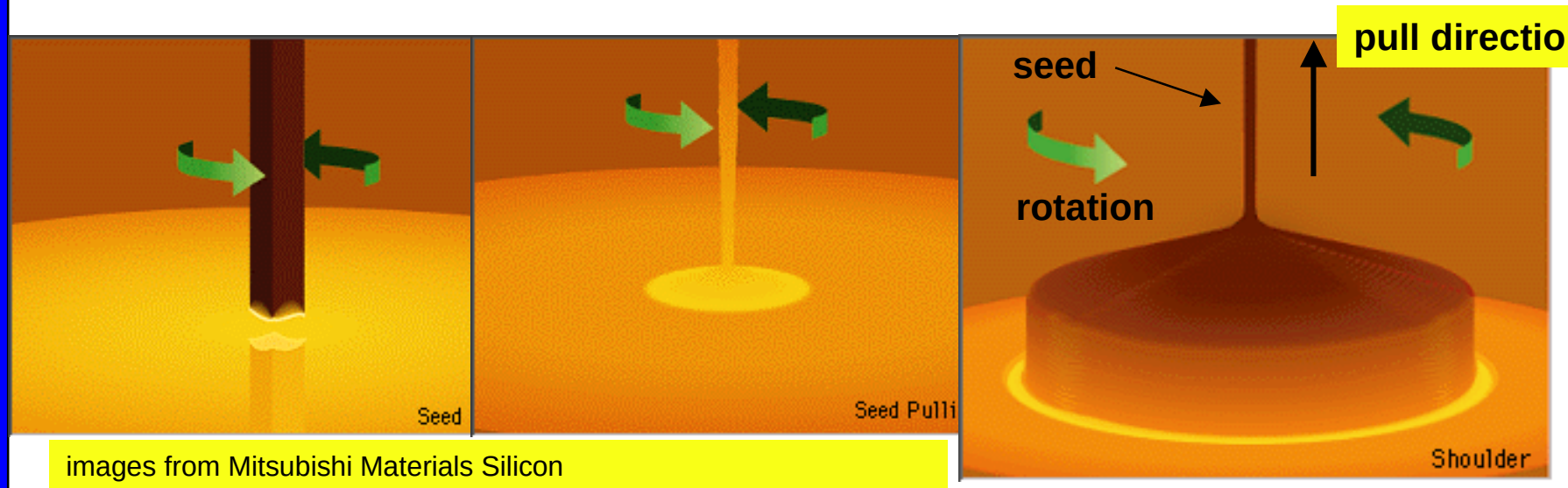
images from Mitsubishi Materials Silicon
http://www.egg.or.jp/MSIL/english/msilhist0-e.html





Diameter control during CZ growth

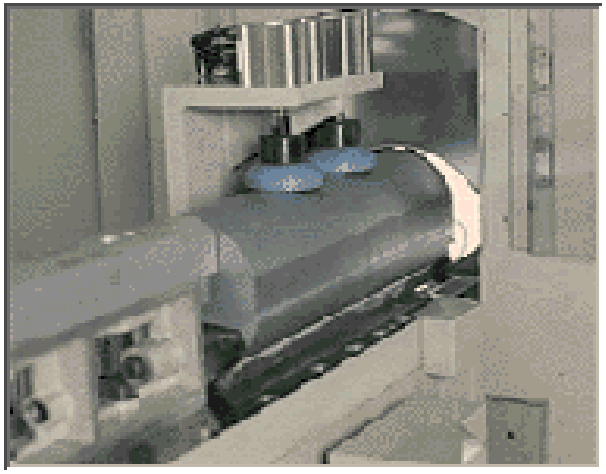
- critical factor is heat flow from liquid to solid
  - interface between liquid and solid is an isotherm
    - temperature fluctuations cause problems!
  - already grown crystal is the heat sink
    - balance latent heat of fusion, solidification rate, pull rate, diameter, temperature gradient, heat flow
    - diameter inversely proportional to pull rate (typically ~ mm/min)

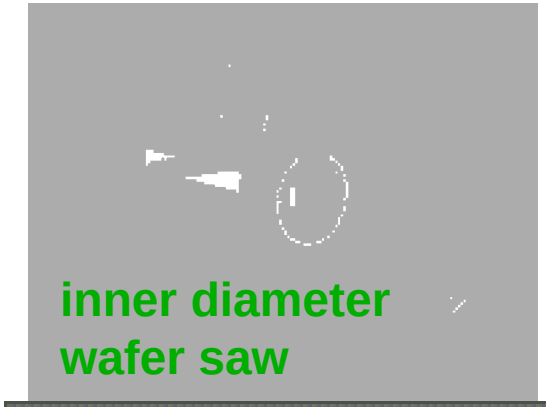


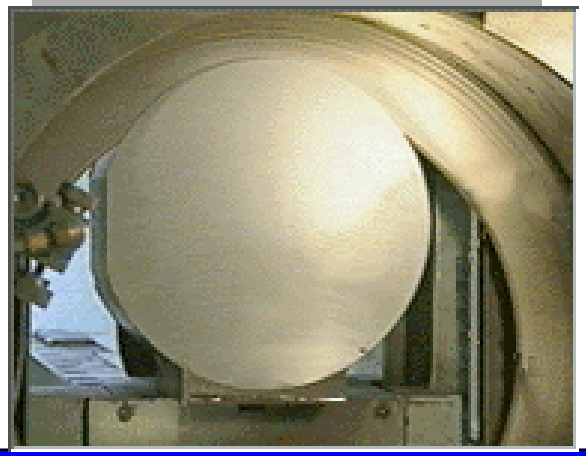
images from Mitsubishi Materials Silicon
http://www.egg.or.jp/MSIL/english/msilhist0-e.html

Wafer preparation

- boule forming, orientation measurement
  - old standard: “flat”perpendicular to <110> direction;
  - on large diameter “notch” used instead







- wafer slicing
  - <100> typically within ± 0.5˚
  - <111>, 2˚ - 5˚ off axis

images from Mitsubishi Materials Silicon
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Wafer prep (cont.)

- lapping
  - grind both sides, flatness ~2-3 μm
    - ~20 μm per side removed
- edge profiling
- etching
  - chemical etch to remove surface damaged layer
    - ~20 μm per side removed
- polishing
  - chemi-mechanical polish, SiO_2 / NaOH slurry
    - ~25 μm per polished side removed
  - gives wafers a “mirror” finish
- cleaning and inspection

Wafer specifications

wafer diam.	thickness	thickness variation	bow	warp
150 mm ± 0.5mm	675μm ± 25μm	50μm	60μm	
200 mm ±				
300 mm ± 0.2mm	775μm ± 25μm	= 10μm		= 100μm

- warp: distance between highest and lowest points relative to reference plane
- bow: concave or convex deformation

Thin film processes

- "grown" films
  - typically "converted" from original substrate material
    - example: SiO2 formed by oxidation of Si substrate
- "deposited" films
  - crystalline, poly crystalline, amorphous
  - electro-deposition
    - not standard IC process
  - liquid phase deposition
    - not standard IC process
  - vapor phase deposition
    - PVD: physical vapor deposition
    - CVD: chemical vapor deposition